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(54) FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

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- (52) U.S. Cl. 713/501; 713/300; 713/503
- (58) Field of Search \_\_\_\_\_\_\_ 713/300, 320, 713/322, 500, 501, 503

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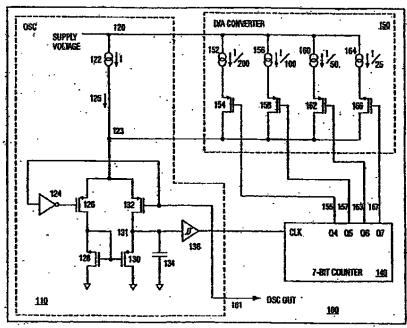
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(57) ABSTRACT

EMI emission is reduced by jittering the switching frequency of a switchird mode power supply. An oscillator with a control input for varying the oscillator's switching frequency generates a jittered clock signal. In one embodiment, the oscillator is connected to a counter clocked by the oscillator. The counter drives a digital to analog converter, whose output is ponnected to the control input of the oscillator for varying the oscillation frequency. In another embodiment, the oscillator is connected to a low frequency oscillator whose low frequency output is used to supplement the output of the oscillator for jittering the switching frequency. The invention thus deviates or jitters the switching frequency of the switched mode power supply oscillator within a narrow range to reduce EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment.

### 32 Claims, 6 Drawing Sheets

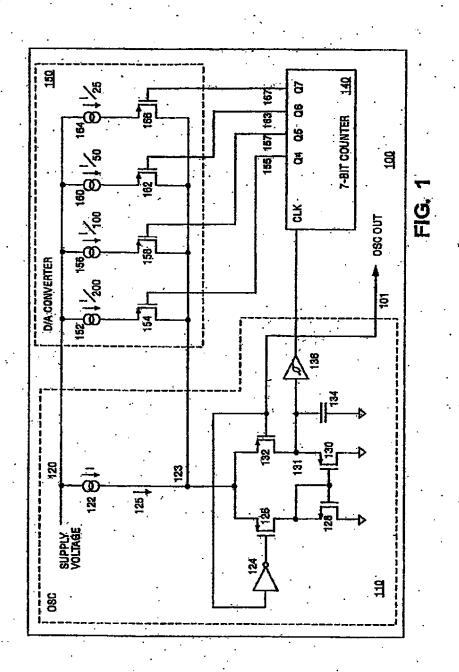




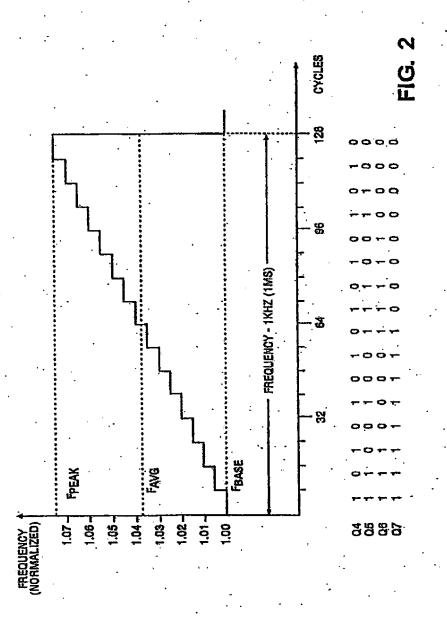
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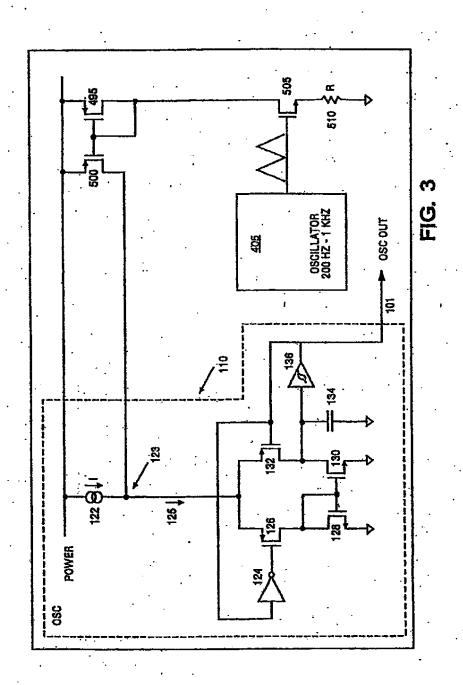


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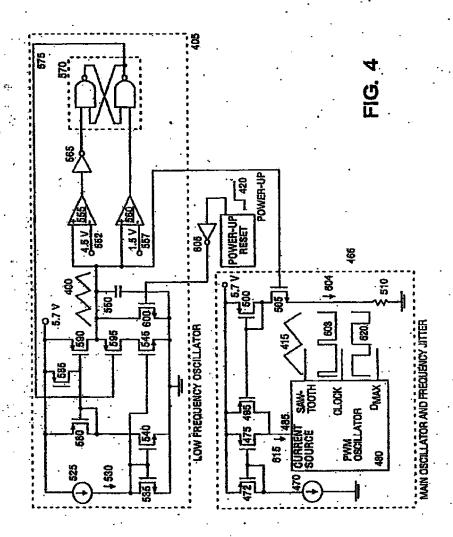
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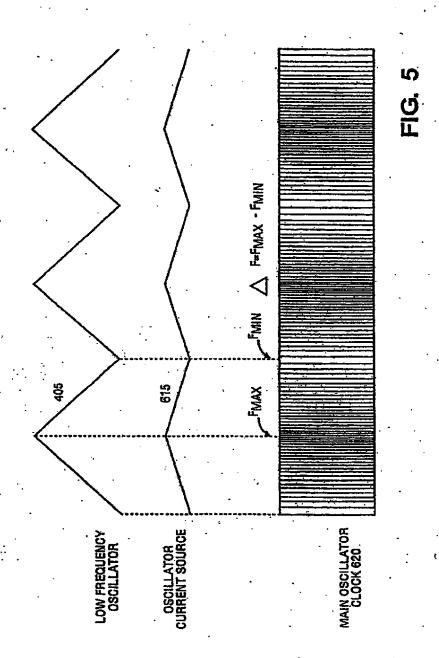


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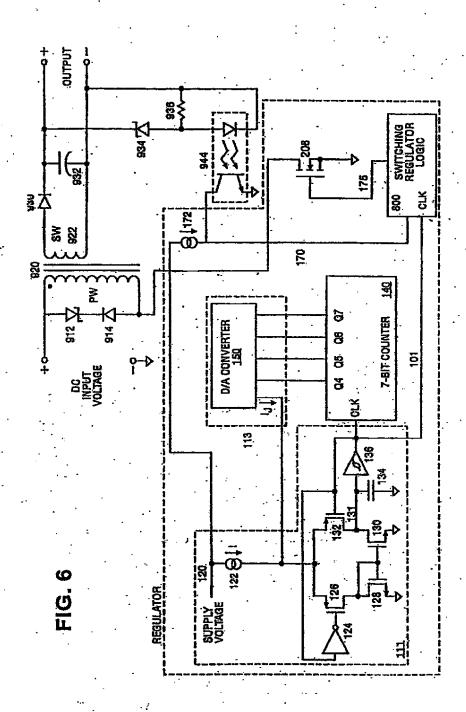
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### FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

### RACKGROUND

The present invention relates to an off-line switched mode control system with frequency jiltering.

Many products rely on advanced electronic components to cost-effectively provide the product with the desired functionally. These electronic components require power regulation circuitry to supply them with a clean and steady source of power. The development of switched mode power supply technology has led to power supplies operating at high frequency to achieve small size and high efficiency. Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternatively a variable frequency (such as in a ringing choke power supply).

Due to the high frequency operation relative to the frequency of an alternating current (AC) power line, switched mode power supplies can exacerbate problems associated with electromagnetic faterference (EMI). EMI moise is generated when voltage and current are modulated by the switching power supply. This electrical noise can be transferred to the AC power line.

hi addition to affecting the operation of other electronics within the vicinity of the power supply by conduction, EMi induced noise on a power line may radiate or leak from the power line and affect equipment which is not even connected to the power line. Both conducted and radiated electrical noise may adversely affect or interfere with the operation of the electronic equipment. For example, EMI noise generated by the switching power supply can cause problems for communication devices in the vicinity of the power supply. 18 Radiated high frequency noise components may become a part of the AC mains signal and may be provided to other devices in the power grid. Further, power supply radiated EMI can interfere with radio and television transmissions.

To address EMI related interference, several specifications have been developed by government agencies in the United States and in the European Community. These agencies have established specifications that define the maximum amount of EMI that can be produced by various classes of electronic devices. Since power supplies generate a major as component of the EMI for electronic devices, an important step in designing such supplies that conform to the specifications is to minimize EMI emission to the acceptable limits of the various specifications.

EMI may be reduced in a power supply by adding so southbers and input filters. These components reduce the noise transferred to the power line and by so doing, also reduce the electric and magnetic fields of noise generated by the power line. While these methods can reduce EMI, they usually complicate the design process as well as increase the 55 production cost. In practice, noise filtering components are added in an ad hoc manner and on a trial-and-error basis during the final design process when EMI is found to exceed the compliance limits specified by the regulatory agencies. This inevitably adds unexpected costs to the products.

Further, extra components can undestrably increase the size and weight of the power supply and thus the resulting product.

### SUMMARY OF THE INVENTION

EMI emission is reduced by fittering the switching frequency of a switched mode power supply. In one aspect, a 2

frequency filtering circuit varies the switching frequency using an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency. A digital to analog converter is consacted to the control input for varying the switching frequency, and a counter is connected to the output of the oscillator and to the digital to analog converter. The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency.

Implementations of the invention include one or more of the following. The oscillator has a primary current source connected to the oscillator control input. A differential switch may be used with first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and one or more comparators may be connected to the junction. The original to analog converter has one or more current source and in the counter. The primary current source may generate a current I and each of the current sources may generate a current lower than I. The current sources may generate binary weighted currents. The largest current sources may generate binary weighted currents. The largest current sources may generate a current which is less than about 0.1:

Is a second aspect, a method for generating a switching frequency in a power conversion system includes generating a primary current; cycling one or more secondary current sources to generate a secondary current which varies over time; and supplying the primary and secondary currents to a control input of an oscillator for generating a switching frequency which is varied over time.

implementations of the invention include one or more of
the following. A counter may be clocked with the cutput of
the oscillator. The primary current may be generated by a
carrent source. If the primary current is I, each of the
secondary current sources may generate a supplemental
carrent lower than I and which is passed to the oscillator
control input. The supplemental current may be binaryweighted. The largest supplemental current may be less than
approximately 0.1 of I.

In another aspect, a method for generating a switching frequency in a power conversion system includes generating a primary relarge, cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and supplying the primary and secondary voltages to a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. Where the primary voltage is V, each of the secondary woltage sources may generate a supplemental voltage lower than V which may be passed to the voltagecontrolled oscillator. The supplemental voltage may be binary-weighted.

In another aspect, a frequency jittering circuit for varying a power supply switching frequency includes an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency; and means connected to the control input for varying the switching frequency.

Implementations of the invention include one or more of the following. The means for varying the frequency may include one or more current sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more current sources. The oscillator may include a primary current source connected to the control

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input; and a differential switch connected to the primary current source. The differential switch may have first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and a comparator may be connected to the innetion. If the primary current source generates a current I, each of the corrent sources may generate a second current lower than the current I, further comprising a transistor connected in each current source connected to the counter. The means for varying the Esequency may include one or more voltage sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more voltage sources. The oscillator may include a primary voltage source connected to the control input; and a differential switch connected to the primary voltage source. The means for varying the frequency may include a capacitor; a current scence adapted to charge the capacitor; and means for alternatingly charging and discharging the capacitor. One or rators may be connected to the capacitor and the means for alternatingly charging and discharging the capaci-

In yet another aspect, a power supply includes a amer, an oscillator for generating a signal having a frequency, the oscillator having a control input for varying. 25 the frequency of the signal, the oscillator including a primany carroal source connected to the control input; a difforcatial switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. The power supply also lactudes a digital to analog conventer conn to the control input, the analog to digital converter having one of more current sources, wherein the primary current source generates a corrent I and each of the current sources enerates a corrent lower than L A-counter is connected to the output of the oscillator and to the entreal sources of the digital to analog convener. Further, a power transistor is connected to the primary winding of the transformer so that when the power transistor is modulated, a segulated power supply output is provided.

In another aspect, a power supply includes a transformer connected to an input voltage. The power supply includes an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the socillator including; a primary current source as connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the fifterential switch; and a comperatur connected to the differential switch. A circuit for varying the frequency is connected to the control input, the circuit having a capacitor; one or more companions connected to the capacitor, one or more companions connected to the capacitor to the current source for alternatingly charging and discharging the capacitor. Further, a power leastsitor is connected to the oscillator and to the primary winding. The power transistor southers is output in providing a regulated power supply

Advantages of the invention include one or more of the following. The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads onergy outside of the bandwidth measured by the EMI measurement equipment. By changing the oscillator frequency back and forth, the average noise measured by the EMI measurement equipment is reduced considerably.

Farther, the invention provides the required jittering without requiring a large area on the regulator ctup to implement a capacitor in a low frequency oscillator. Further, the invention minimizes effects caused by leakage carrent from transistors and capacitors associated with a low frequency oscillator. Thus, the filtering operation can be maintained even at high temperature which can increase carrent leakage.

Additionally, the invention reduces the need to add extra noise filtering components associated with the EMI filter. Therefore a compact and inexpensive power supply system can be built with minimal EMI emissions.

### BRIEF DESCRIPTION OF THE DRAWINGS .

FIG. 1 is a schematic diagram of a digital frequency filtering device.

FIG. 2 is a plot illustrating the operation of the device of FIG. 1.

FIG. 3 is a schematic diagram of an analog frequency filtering device.

FIG. 4 is a schematic diagram of an implementation of the device of FIG. 3.

FIG. 5 is a timing diagram Illustrating the operation of the frequency litter device of PIG. 4.

FIG. 6 is a schematic diagram of a switched mode powersupply in accordance with the present invention.

### DESCRIPTION

FKG. I shows a digital frequency jittering circuit 100. The digital frequency jittering circuit 100 has a primary oscillator. 110 which provides a chock signal to a counter 140. The primary oscillator 110 typically operates between 100 kHz and 130 kHz. The counter 140 can be a seven bit counter. Each output of counter 140, when clocked by primary oscillator 110, represents a particular line interval. The soutputs of the counter 140 are provided to a series of frequency jittering current sources 150. The outputs of the series of frequency jittering current sources 150 are presented to the primary oscillator 110 to vary its frequency, as will be described below.

Primary oscillator 110 contains a primary current source 122 which provides a primary courses (denoted as f) to node 123. Current 125 to the node 123 is provided to the source of MOSPET transistors 126 and 132. The drain of MOSPET consistor 126 is connected to the drain of an n-channel MOSFET transistor 128. The source of transistor 128 is grounded, while the gate of the transistor 128 is connected to its drain. The gate of the transistor 128 is also connected. to the gate of an n-channel MOSPET transistor 130. The source of the transistor 130 is grounded while the drain is connected to the drain of the MOSFET transistor 132 at a node 131. Transistors 126, 128, 130 and 132 form a differradial switch. The output of comparator 136 is connected to the gate of the transistor 132 and to an inverter 124. The couput of invector 124 is connected to the gate of wassistor 126. The comparator 136 has an input which is connected to node 131 and to a capacitor 134. In combination, the transistors 126, 128, 130 and 132, capacitor 134, inverter 124, current source 122 and comparator 136 form an oscillator. The comput of the comparator 136 is provided as an oscillator output OSC\_OUT 161 and is also used to drive the clock input of counter 140.

Counter 140 has a pharality of outputs Q1-Q3 (not shown) which are not used. The remaining outputs Q4-Q7 are connected to a digital-to-analog (D-to-A) converter 150, which may be implemented as a series of frequency jittering voltage sources or current sources. A Q4 output 155 is connected to the gate of a p-channel MOSFET transistor

154. A Q5 output 157 is connected to the gate of a p-channel MOSFET transistor 158. The Q6 output 163 is connected to the gate of a p-channel MOSFET transistor 162, and Q7 itout 16? is connected to the gate of a p-channel MOSFET transistor 166. When D-to-A converter 150 is viewed as a 😁 plurality of current sources, the source of transistor 154 is connected to a jittering content source 152, which provides a current which is leasth of the current I generated by the current source 122. The source of MOSFET transistor 158 is cled to a carrent source 156 which provides a carrient 10 that is Viewth of the carrent i. The source of the MOSPET. istor 162 is connected to a jittering current source 160 which provides a current that is Yath of L Finally, the source of the MOSPHT transitior 166 is connected to a jiltering consent source 164 which provides a current that is 1/25th of 15 the content L. The corrent sources 152, 156, 168 and 164 are binary-weighted, that is, the current source 164 provides twice the current provided by the current source 169, the current source 160 provides twice the current supplied by the current source 156 and the current source 156 provides an twice the current provided by the current source 152.

Further, in one embodiment, the largest current source 184 may supply no more than 10% of the current I provided my current source 122. The drain of transistors 154, 158, 162 and 166 are joined together such that the 25 supplemental frequency littering current sources of the D-to-A converter ISB can be provided to supplement the primary current source 122.

During operation, at every night clock cycles, the counter output Q4 on line 155 changes state. Similarly, at every 16 clock cycles, the output Q3 on line 157 changes state and at every 32 clock cycles, the output Q6 on line 163 changes state, and every 64 clock cycles, the output Q7 on line 167 changes state. The comic counting cycle thereafter repeats

Each time the output Q4 on line 135 is low, transistor 154. is turned on to inject current in the amount of 1/200 to node 123 so that the total correct 125 is 1.005i. Similardy, each time that the output Q5 on line 157 is low, transistor 158 is ed on to inject current in the ampunt of 1/100 to node 123. so that the total carrent 125 is 1.011. Further, each time that output Q6 on fine 163 is low, transistor 162 is turned out to inject current in the amount of 1/50 to node 123 so that the total exceed 125 is 1.021. Finally, each time that the output Q7 on line 167 is low, the transistor 166 is termed on to inject current in the amount of 1/25 to node 123 so that the total current 125 is 1.041.

Additionally, when combinations of outputs Q4-Q7 are turned on, the outputs of the respective current sources 152, 39
156, 160 and 164 are added to the output of current source 122 to vary the frequency of the primary oscillator 110. In this manner, counter 140 drives a phreality of current sources to inject additional current to the main current source 122 such that the frequency of the primary oscillator, 118 is 55

The filtering operation of the embodiment of FIG. 1 is further illustrated in a chart in FIG. 2. A normalized operaling frequency is plotted on the y-axis while the counting cycle as shown by the counter outputs Q4-Q7 is plotted on he x-axis. As shown in FIG. 2, as the counter counts unward to the maximum count of 128, the peak switching frequency is achieved. This peak switching frequency is normalized to be about 1.075 times the base switching frequency. Further, on average, the switching frequency is hetween 1.03 and a 1.04 times the base switching frequency. Time, the embedi-ment of FIG. 1 deviates the switching frequency of the

oscillator within a narrow range. This deviation reduces EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment such that the noise measured by the EMI test equipment is reduced considerably.

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FIG. 3 shows an analog frequency jittering circuit. More co-pending U.S. application Set. No. 09/080,774, can'tled "OFFLINE CONVERTER WITH INTEGRATED SOFT START AND FREQUENCY LITTER," filed on May 18, 1998, the content of which is hereby incorporated by reference. In FIG. 3, the primary oscillator 110 provides an oscillator output on fine OSCOUT 101. An analog low frequency oscillator 405 is also provided. Primary oscillator 110 typically operates between a range of 30 to 300 kHz. while the low frequency oscillator 405 typically operates between a range of 5 Hz to 5 kHz. As discussed above, the switching frequency of the primary oscillator 110 is determined by the amount of current the primary oscillator uses to charge and discharge capacitor 134. The low frequency oscillator 405 varies this current within a narrow range to jitter the frequency of the primary oscillator 110.

The output of low frequency oscillator 405 is provided to a MOSFET transistor 505 connected to a resistor 510 and a current mirror including transistors 495 and 500. Transistor 500 is connected to node 123 so that extra current can be added to current source 122 feeding the primary oscillator. In this manner, the frequency of the primary oscillator 110 is shilted around a narrow range to reduce the EMI noise.

FIG: 4 shows a more detailed implementation of FIG. 3. As shows therein, main oscillator 465 has a carrent source 470 that is mirrored by current mirror transistors 472 and-475. Miris oscillator drive current 615 is provided to current source input 485 of oscillator 480. The magnitude of the current input into current source input 485 determines the frequency of the oscillation signal 415 provided by oscillator 480. In order to vary the frequency of the oscillation signal 415, an additional current source 495 is provided within the main oscillator 465. The current source 495 is mirrored by street source mirror 500.

The current provided by current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main escillator transistor 505. As the magnitude of frequency variation signal 400 increases, so does the voltage at the source of main oscillator transistor 505 due to the increasing voltage at the gate of the transistor 505 and the relatively constant voltage drop between the gate and source of the transistor 505. As the voltage at the source of transistor SDS increases, so does the current 664 flowing through the resistor 518. The current flowing through the resistor 510 is the same as the current flowing through additional current source 500 which mirrors transistor 495.

Since the frequency variation signal 400 is a triangular raveform having a fixed period, as shown, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency will linearly use to a peak and then fall to its lowest value. In this way, the current \$15 provided to current source input 485 of the oscillator 480 is varied in a known fixed range that allows for an easy and accurate frequency spread of the high frequency current. Further, the variance of the frequency is determined by the magnitude of the current provided by carreat source mirror 500, which is a supction of the resistance of the resistor 510.

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Frequency variation circuit 485 includes a current source 525 that produces a fixed magnitude current 530 that deletmines the magnitude of the frequency of the frequency must be suggested to the content 530 has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude correst. If such variable current is generated, the frequency spread is not fixed in time but varies with the unagained of current 530. The fixed magnitude current 530 is fed into first transistor 535, mirpored by second transistor 540 and third transistor 545. The frequency variation signal 400 is generated by the charging and discharging of the capacitor 550. Frequency variation circuit capacitor 550 has a relatively low capacitance, which allows for integration into a monohithic chip in one embodiment of low frequency oscillator 405. The frequency variation signal 400 is provided to upper limit comparator 555 and lower limit comparator 568. The output of upper limit comparator 555 will be high when the magnitude of the frequency variation signal 400 exceeds the upper threshold voltage on line 552 which is about 4.5 volts. The output of 20 vosage an use 324 which is about 1.5 volt. The volte of lower Huist comparator 560 will be low when the magnitude of frequency variation signal 400 drops below lower threshold voltage on line 557 which is about 1.5 volts. The output of apper limit comparator 555 is provided to the frequency variation circuit inverter \$65 the output of which is provided to the reset input of frequency variation carean latch 570. The set input of frequency variation circuit latch 570. receives the output of lower limit comparator 560.

In operation, the output of lower limit comparator 560 will be maintained high for the majority of each cycle of an frequency variation signal 400 because the magnitude of frequency variation signal will be maintained between the upper threshold on line 552, 4.5 volts, and lower threshold on line 557, 1.5 volts. The output of upper limit comparator 555 will be low until the magnitude of frequency variation 35 signal 400 exceeds upper level threshold on line 552. This means that the reset input will receive a high signal when the magnitude of the frequency variation signal 400 rises above the upper threshold signal on line 552.

The charge rigarl 575 critical by frequency variation a circuit latch 570 will be high until the frequency variation signal 400 exceeds the upper threshold limit signal on line SSZ. When the charge signal 575 is high, transistors 585 and 595 are turned off. By turning off transistors 583 and 595, carrent can flow into the capacitor 559, which steadily as charges capacitor 559 and increases the magnitude of fre-quency-variation signal 400. The carrent that flows into the capacitor 550 is derived from current source 525 because the rest through transistor 590 is mirrored from transistor 550, which in two is mirrored from transistor 535.

During power up, when power up signal 420 is low, the output of inventer 605 is high, which terms on transistor 600, sing frequency variation signal 400 to go low. The pacacy variation signal 400 starts from its lowest level to perform a soft start function during its first cycle of opera- 55

Referring to FIGS: 4 and 5, FIG. 5 shows the operation of the analog frequency jittering device of FIG. 4. In FIG. 5, a frequency variation signal 485 is provided to the main occiliator 465. The magnitude of the current 615 is approximainly the magnitude of the frequency variation signal 485, less the threshold voltage of transistor 585, and divided by the resistance of the resistor 510 ples the magnitude of the arrent produced by the current source 475. The corrent 615 varies with the magnitude of the frequency variation signal 65 405. The variation of the current 615 in turn varies the frequency of the oscillator clock."

Referring now to FIG. 6, a switched mode power supply is shown. Direct current (DC) input voltage is provided to a Zener diade \$12 which is connected to a diade \$14. The diodes 912-914 together are connected in series across a primary winding of a transformer 920. A secondary winding 922 is magnetically coupled to the primary winding of transformer 920. One terminal of the secondary winding 922 is connected to a diode 930, whose output is provided to a capacitor 932. The junction between diode 930 and capacitor 932 is the positive terminal of the regulated output. The other terminal of capacitor 932 is connected to a second terminal of the secondary winding and is the negative terminal of the regulated output. A Zener diode 934 is connected to the positive terminal of the regulated output. The other end of Zener diode 934 is connected to a first end of a light emitting diode in an opto-isolator 344. A se and of the light-emitting diode is connected to the negative terminal of the regulated output. A resistor 936 is connected between the negative terminal of the regulated output and the first end of the light-emitting diode of opto-isolator 944.

The collector of the opto-isolator 944 is connected to current source 172. The output of correct source 172 is provided to the switching regulator logic 800.

Connected to the second primary winding terminal is the power transistor 206. Power transistor 206 is driven by the switching regulator logic 800. Switching regulator logic 800 receives a clock signal 101 from an oscillator 111. A counter 140 also receives the clock signal 101 from the primary escillator, 111. The outputs of counter 140 are provided to D-to-A converter 150, which is connected to oscillator 111 for fittering the oscillation frequency. Alternatively, in lieu of counter 149 and a D-to-A converter 159, an analog low frequency jittering oscillator may be used.

The foregoing disclosure and description of the invesre illustrative and explanatory thereof, and various changes in the size, shape, materials, components, circuit elemns and contacts, as well as in the details of the illustrated circuitry and construction and method of operation may be made without departing from the spirit of

What is chimed is:

- 1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:
- an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency
- digital to analog converter complet to the control input for varying the switching frequency; and
- a counter coupled to the output of the oscillator and to the digital to analog converter, the counter crusing the digital to analog converter to adjust the control input and to vary the switching frequency.
- 2. The circuit of claim 1, wherein the oscillator further comprises a primary current source coupled to the oscillator control input.
- 3. The circuit of claim 2, further comprising a differential switch, including:
- first and second transistors coupled to the primary current
- a third transistor coupled to the first transistor; and
- a fourth transistor coupled to the second transistor at a
- 4. The circuit of claim 3, further comprising a capacitor coupled to the junction.
- 5. The circuit of claim 3, further comprising one or more comparators coupled to the junction.

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6. The circuit of claim 2, wherein the digital to analog converter has one or more secondary current sources.

7. The circuit of claim 6, further comprising a transistor coupled between each secondary current source and the

8. The circuit of claim 5, wherein the primary current source generates a current I and each of the secondary current sources generates a current lower than L

9. The circuit of claim 8, wherein the accordary current sources generate binary weighted currents.

19. The circuit of claim 8, wherein the largest secondary current source generates a current which is less than about 0.1 of I

11. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary current

cycling one or more secondary current sources to generate a secondary current which varies over time; and

combining the secondary current with the primary current to be received at a control input of an oscillator for 20 generating a switching frequency which is varied over

12. The method of claim 11 further comprising the step of clocking a counter with the output of the oscillator.

13. The method of claim 11 wherein the primary coursest 25 generated by a current source

14. The method of chim 11 wherein the primary current is I and each of the secondary current sources generales a supplemental current lower than I, and further comprising sing the supplemental carrent to the oscillator control

15. The method of claim 14 further comprising binary-

reighting the supplemental carrent.

16. The method of claim 14 wherein the largest supple-

ental current is less than approximately 0.1 of I.

17. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary voltage;

cycling one or most secondary voltage sources to generate secondary voltage which varies over time; and combining the accordary voltage with the primary voltage to be received at a control isput of a voltage-controlled oscillator for generalities a switching frequency which is varied over tis

18. The method of claim 17 further comprising clocking 45 a counter with the output of the oscillator.

19. The method of claim 17 wherein the primary veltage is V and each of the secondary voltage sources generates a supplemental voltage lower than V, farther comprising passing the supplemental voltage to the voltage-controlled oscil-

20. The method of claim 19, wherein the supplemental voltage is binary-weighted.

an oscillator for geocrating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency; and

caus coupled to the control input for varying the switching frequency, including:

one or more current sources coupled to the control input; and

a counter coupled to the output of the oscillator and to the DOC OF MORE Climent Sparces.

22. The carcuit of claim 21 wherein the oscillator further

a primary current source coupled to the control differential switch coupled to the primary sour repled to the control input; and

23. The circuit of claim 22 wherein the oscillator further

first and second transistors coupled to the primary current

a third transistor coupled to the first transistor, and

a fourth transistor coupled to the second transistor at a inaction.

24. The circuit of claim 22 further comprising a capacitor and a comparator coupled to the junction

25. The circuit of claim 22 wherein the primary carrent source generates a current I and each of said one or more surrent sources generates a current lower than I.

26. The ciscuit of claim 22 wherein the primary content source generales a current I and each of said one or more carrent sources generales a second current lower than the current I, finisher comprising a transistor coupled to each current source connected to the counter.

27. The circuit of chim 21 farther comprising a transistor compled to each current source and to the con-

28. The circuit of claim 21 wherein the oscillator further

a primary voltage source coupled to the control input; and a differential switch coupled to the primary voltage

29. The circuit of claim 21 wherein the meses for varying the frequency further comprises:

a capacitor; and

a current source adapted to charge and discharge the cupacitor.

39. The circuit of claim 29 further comprising:

one or more comparators coupled to the capacitor, and means coupled to the capacitor for alternatingly charging and discharging the capacitor.

31. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including

a primery current source completi to the control input; a differential switch coupled to the primary current

a capacitor coupled to the differential switch; and a comparator coupled to the differential switch:

a digital to analog converter coupled to the control input, the digital to analog converter having one or more current sources, wherein the primary current source generates a correst I and each of said one or more current sources generates a current lower that I;

a compler complete to the output of the oscillator and to the current sources of the digital to analog converter, and 21. A frequency filtering circuit for varying 2 power 55 2 power transistor coupled to the oscillator and to one supply switching frequency, comprising:

Leminal of the primary winding, the power transistor modulating its cutput in providing a regulated power supply output.

32. A power supply having a transformer complet to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input; a differential switch coupled to the primary current SOMECE"

- a capacitor coupled to the differential switch; and a comparator coupled to the differential switch
- a circuit for varying the frequency, the circuit coupled to the control input, including: a capacitor,
  - a current source adapted to charge and discharge the capacitor;
  - coupled to the current source for alternatingly charg-ing and discharging the capacitor; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,249,876 B1 DATED : June 19, 2001

Page 1 of 1

DATED: June 19, 2001
INVENTOR(S): Balakrishnan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

### Column 10.

Line 2, please insert — current — after "primary".

Line 3, please delete "wherein the oscillator further" and insert — wherein the differential switch further —

Signed and Sealed this

Nineteenth Day of February, 2002

Atleste

JAMES E. ROGAN

Director of the United States Perent and Frederical Of

## PX 2

### United States Patent [19]. Balakirshnan et al.

[45] Date of Patent:

SOFTSTART AND FREQUENCY JITTER	[54]	OFFLINE CONVERTER WITH INTEGRATE SOFTSTART AND FREQUENCY JITTER
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- [21] Appl. No.: 05/060,774
- (ZZ) Filest. May 18, 1998 HRSK 3/617 377/72; 327/631; 327/544 377/72, 173, 377/72, 173, 377/74, 175, 176, 330, 531, 544

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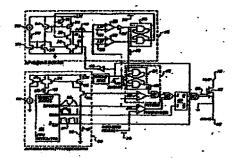
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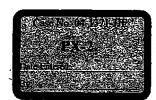
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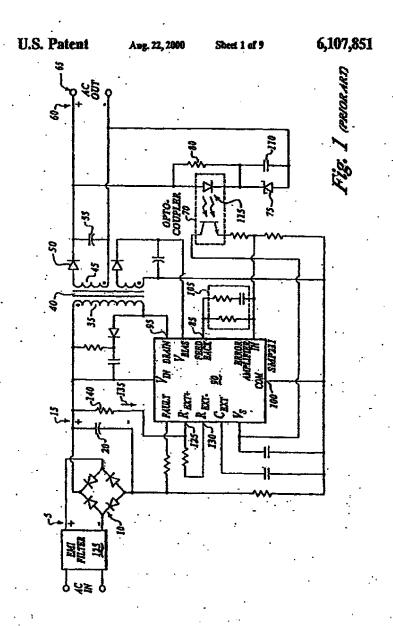
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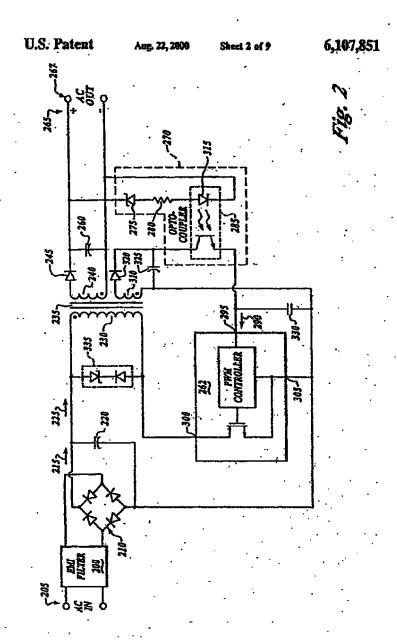
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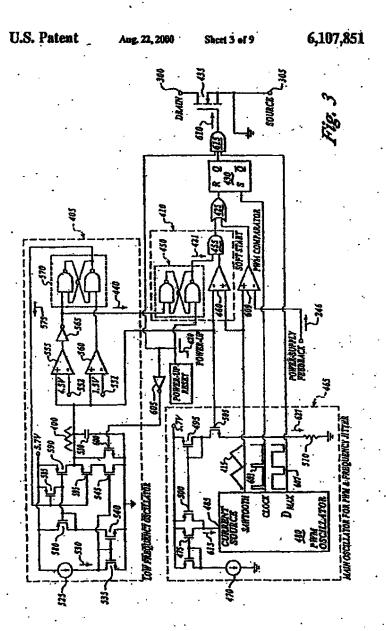
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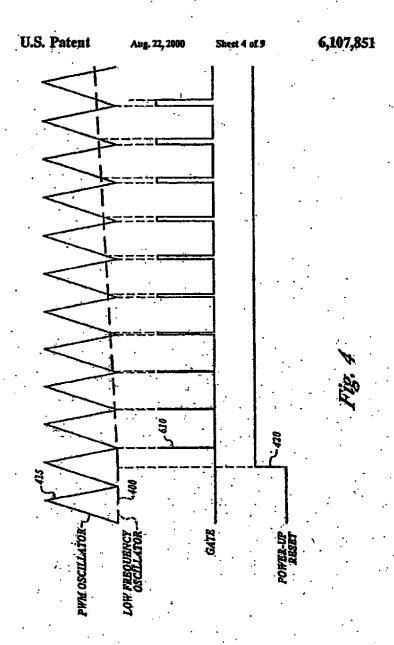




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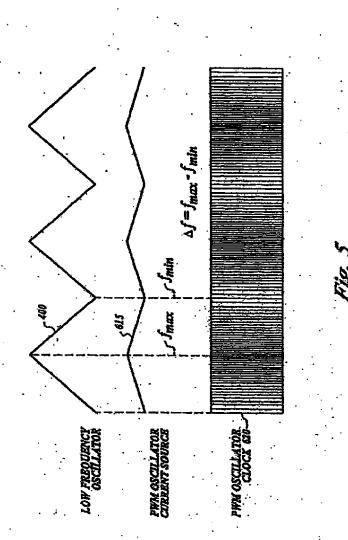


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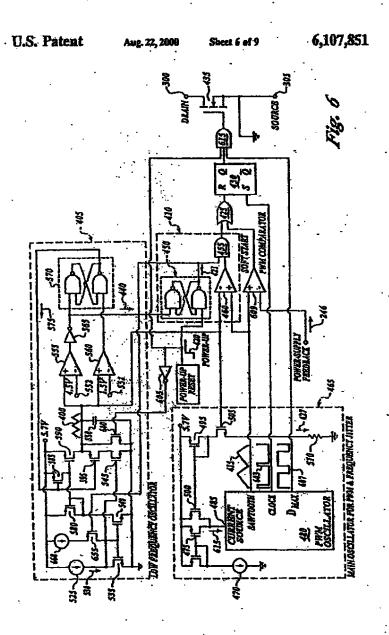


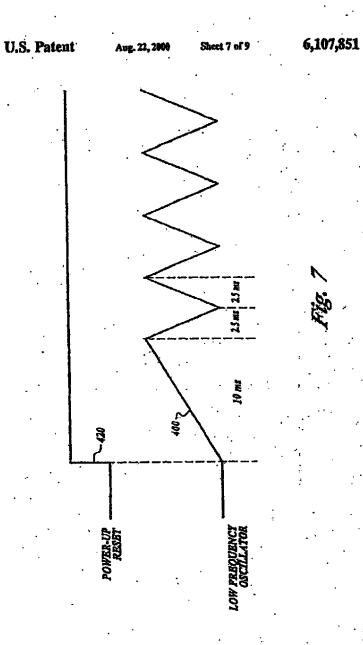
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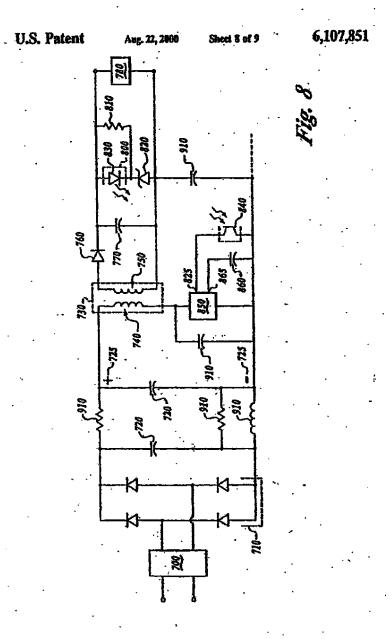
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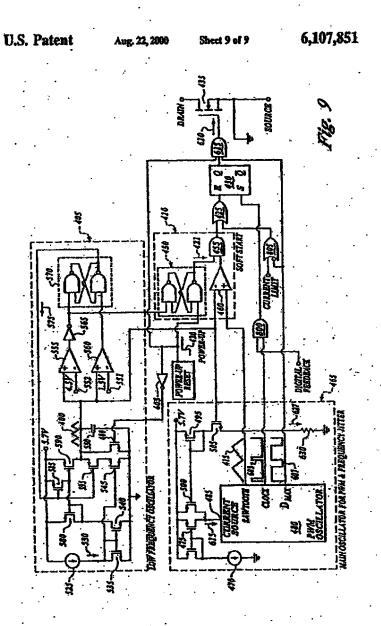


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### OFFLIRE CONVERTER WITH INTEGRATED SOFTSTART AND PREQUENCY JITTER

### BACKGROUND

e pertains to the field of rings to the argulation of

vices, are known, two grants or power washing of the cho-hin the output voltage, control or power washing drings for efficient and asle operation of the cho-dening for efficient and asle operation of the cho-mannal, or power of the power supply within a regulated sange are also known. Them switches utilize are neciliator and existed circularly to very the switching [requirecy of operation of the switch, and store from regulated the general curvature or voltage

caronic stocks whiches of this an oscillator and related circularly to vary the switching Impanenty of operation of the switch, and therefore regulated the power, extrant or wohage that is stoppide by the power stoppic.

A problem with milliting pulse withit modulated switches is that they operate at a relatively high frequency compared to the furtherney of the AC switce voltage, which remain in a high frequency signal being generated by the gover analyst and the power apply. This high frequency signal is injected back into the AC matter input so obsciousness a component of the AC sation signal. The high frequency signals are also estimated by the power supply. These high frequency signals are also estimated by the power supply, and he fact are the highest contributors to the EM of the power pumply. The EMI generated by the power supply can cause problems for communications devices in the vicinity of the power supply and the high frequency signal which becomes a component of the AC sation signal which becomes a component of the power supply that the state of the AC sation signal which becomes a component of the power supply that the contributors for those the power supply that the contributors in the vicinity of the power supply do the power supply that the power supply that the contributors is the two transmissions that we transmissions that we transmissions and televisions it and the states.

To combat the problems of EMI, saveral specifications

The combut the problem of Erick, neveral specifications we been developed by the Federal Convisionations Consistentiation (PCC) in the United States and the European nationally (EC) have established specification that specify: panelingly research of Maria that the Consistential Research of Maria that the the plantatum encount of EMM that can be produced by classes of leterosis devices. Since power stypiles groweds a major component of the EMM for electronic devices, as important step in designing a power stypily is involved, the EMM provided by the power stypily is haveln with the acceptable limits of the various standards. Since, a power stypily can be stillard in gauge different countries of the world, the EMM produced should be writted for unout students femile, worldwick to allow for minimum stillention of the resuscence aments.

nt of the EMI filter is in large (

results from operation of the power supply at start

and the secondary side components of sixess caused by the quantum insuch weard life of the power supply and in power supply because the searchose nearly seed at the power supply to a found consents will be greater than required for normal operation. inest canous will be greater to require for normal operation. Further, when the pulse width m

Further, when the pulsa width modulated awhich conducts for the maximum possible amount of time in each cycle of operation the wilkings, current and power at the owners of the power supply rises angidly. Since the feedback circuit of the power supply of the modes not enspond as fast as the operating frequency of the switch, the rapid time of the related, current and power will often result in an overshoot of the maximum voltage in the regulation range which will cause descript to the device being supplied power by the power supply. Relatings to FIG. 1 a known power supply that alterapts to radiatings: EMI and suchase attempts the salesting respirate to the power supply.

to exhibition: EMI and achieve stratop strator is depicted. A sectilist 10 rectilists the filtered AC statios voltage 5, from the EMI filter 12A, legacity by the AC station to generate a medical voltage 15. Power supply expected 20 than generates a substitutinity DC voltage with a single component. The actified voltage 15 with ripple component is provided at the primary winding 35 of structionner 40 that is used as provide power to accordary winding 45. The actignt of accordary winding 45 is provided to accordary sentitive 30 and secondary capacities 55 that provide a secondary DC voltage 40 at the power supply unique 65 to 46s device that is coupled to the power supply unique 65 to 46s device that is coupled to the power supply

to the province supply.

In other to making the secondary DC voltage within a register reage a feedback loop including to explority see the secondary seems of t stater those 73 and a sentiment resistor are provides a signal subficiative of the voltage at the power supply output (5 to feathert pin 85 of pulse width muchated switch 90. The voltage angularde at the feathert terminal is utilized to vary the class eyects of a switch coupled between the dwist learning 35 and common screenful 180 of the pulse with modelshed switch 90. By varying the duty cycle of the arther the switch the swarper current flowing through the principal voluntion and therefore the manner steady by the transportations. modelskid sweich Per. By varying the easy open or too switch the average extend flowing through the primary winding and therefore the energy stood by the transformer 40 which is then control the power supplied to the power supply output 45 is large within the arguined range. A companion circuit 18% is coughed to the feedback pin 45 is order to lower the beadwidth of the frequency of opera-

in older to lotter the beadwidth of the trequency or opera-dos of the pulse width mediator. lareds, concents are uniformly of soft that consider MR. Soft start functionally is termed to be a furciously that reduces the innest concent at start up. Mr. functionality that recitions the remain concents at start up. At this impose a circuite begins to have through functional recition 10 and thereby into such state operation 110. As the voltage of 30st start capacitor 110 honomers abovely, content will flow through light embring diods 115 of optionsyler 70 thereby controlling the duty cycle of the switch. Onto the voltage of the soft start especifier 110 rancher the ownerse breakdown voltage of some sibest capacitor 110 rancher the ownerse breakdown voltage of some sibest of 50 rate of will flow through super clode 75. The approach described above with raduce the issuate cannot cannot be power supply, however,

of some same selfd output by the power supply an Ehd or 120 in william. Additionally, pulse width studelisted teb 90 is equipped with inequancy escillation regularity To reduce the EMI output by the power supply as EMI fiber 12D is williand. Additionally, pulse width studelisted to switch 90 is equipped with fisquency exciliation terminals 123 and 130. Frequency oscillation terminals 123 and 130 percent of the second process of the expense of the specific point of the request of the specific point of the specific

problem associates with the EMI reducibes accessed which expect to FEG. I is that the right confronces have varioused to FEG. I is that the right confronces have varioused do to variotious in the line wellige and at least. Additionally, since the ripple may vary, design the component value of EMI exister 14th is difficult to remain and conveyendingly design of the power amply mean problematic.

### SUMMARY OF THE INVENTION

SUMMARY OF THE INVENTION

In our conditions the present invention comprises a price width anothering switch comprising a switch that above a signal to be transmitted between a first terminal and a second demained according to a clive signal. The pulse width modelated switch who comprises a frequency variation circuit that provides a frequency variation circuit that provides a frequency variation signal having a frequency that varies within a brequency request according to the frequency variation signal. The oscillator thather provides a frequency variation signal. The oscillator thather provides a maximum date varies within a brequency state of the provides as a frequency variation signal. The oscillator thather provides a frequency variation signal. num duty cycle signal compilities a lest state and a letter. The pulm width wedeleted circuit further for a drive circuit that provides the drive signal when citamin duty cycle signal is in the first state and a win of the cocilitation signal is below a variable tel level.

are the above completes are excitator that provides a new lame, a duty cycle in gand comprising an entent as and an efficial, a drive circuit that provides the trive signal, and a soft start circuit that provides a signal instructing and drive circuit to disable the drive signal during at less a portion of acid co-state of the maximum desty cycle.

provides the drive sig a signal incis signal.

Select a redships circuit com-signal to be transmitted between the selection of the select unnical according to a drive agoal, a frequent countries to a foregoing to a drive agoal, a frequen-cious dut provides a frequency variation signal, clicuit that provides a thire signal for a max puriod of a time destation sycla. The bine des-cycle varies according to the for-

As object of an expect of the present invention is discard to a pulse width modeland switch that has integrated soft start capabilities.

start cambilisms.

Another object of an aspect of the presset invention is directed forward a pulse width anotherand awards that has integrated frequency vertation capabilities.

Yet souther object of an aspect of the present invention is directed forward a pulse width modelated switch that has a subsect of the formation with the large statement with the capabilities and integrated integrated frequency warmion expandition and integrated and start capabilities.

A futher object of an espect of the present invention is directed toward a low cost regulated power supply that has both and stant and firequency variation capabilities. This and other objects and espects of the present inven-tions are temple, depicted and described in the drawings and the description of the invention contained herein.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 5 is a function power supply utilizing a pulse width modulated solucit, and external soft start, and incorrecy jitus functionality.

FIG. 7 is a presently perfected power supply utilizing an poles width modulated switch according to the present invention.

FIG. 3 is a presently preferred pulse width modulated switch according to the present investor, the present investor of the FIG. 4 is a finding Diagram of the 20th start operation of the presently professed judge width modulated switch according to the present investigate.

to the present invention, Fig. 3 is a similar diagram of the frequency jilter operation of the presently preferred galax width modulated savieth according to the present fovertion. Fig. 5 is no adverted presently preferred judge width modulated awhith according to the present invention. Fig. 7 is a fluid gringram of the special invention of the abstraction presently preferred pulsa width modulated awhith of Fig. 5 according to the present presently preferred pulsa width modulated awhith of Fig. 5 according to the present, inventions.

FIG. 8 is a presently professed power copyly within regulation clocks according to the present invention. FIG. 9 is a presently professed segulation clouds accord to the present invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 2, EMI Star 200 is complet to se AC mains voltage 203. The AC stains voltage 200 is recitind by recifier 218. The recified voltage 215 is provided to power

itage 225 is provided to style 235 which stores the

urding to a duty cycle, that is in part determined by beach from the power supply output 267. Patha width infested switch 262 is a switch that operation according to a width modifiated coulod. Feichback so this pulse width 262 is accomplished by salization of back circuit 276, which is presently preferred to compare the could 276, which is presently preferred to compare 285. Opinionsplus 285 provides a feetback with 390 to free-back terminal 295 of pulse width mode-sization 276, which 262. The feetback terminal 295 of pulse width mode-sization 276 which 262. The feetback terminal terminal 300 could be switch 262. The feetback terminal 265 of pulse width mode-sization 260 and the results in the feetback terminal 300 could be switch 262.

comest or power of the power supply.

Led for feedback, the present levention is also cap
and for feedback, the present levention is also cap

critics of the current supplied at the feedback tension; whilesed to supply bine power for operation of the which modulated switch 262. The monistrict of the topes at the feedback insufand 255 is wittend to I fee days cycle of the pulse which modulated switch for the own.

ctrical import and/or computed surject 762. They need w الحراة اعتور

powers, those less than approximately common made choice which is office its EMS litter 128 can be replaced with ind

to first of FIG. 2 the strinber of components within schools. This produces the overall cost of the power sop as well as reducing its time. Referring to FIG. 3, Insquency variation signal 40 dilited by the pubes widels mechanism awhich 26% to ver-winding Insquency within a frequency range. The peacy variation signal 40% is provided by Insquency va-tons circuit 44%, which preferribly ecosphics as excell that construct a lower fearment than print accritions. nue curcus was, which preteribly con-the operates it a lower frequency that i The frequency variation signal 400, by he a transpire waveform that preferrably four point five (4.5) woke and one poi Although the presently preferred freque-400 is a minigative waveform, alternate

All in a kingalar weveform, alternals frequency variation signals much as cases signals, consister output signals or other signals that very in magnitude during a fixed period of time tamp be utilized as the frequency variation signal.

The frequency variation, eigent, 400 is provided to not start circuit 418. Disting operation soft start circuit 418 and provided with pulse within movitation frequency signal 415 and provided with pulse within movitation frequency signal 416 and provided with pulse within movitation frequency signal 416 post signs 470 reactives by post value for the first stars. Soft itself excellent by once in provided with the signal 470 reactives by post value for the first stars. Soft itself excellent 410 will instead outlier to the in \$40.57827. Soft start circuit 410 will instead switch 435 to come conduction when the roll start qualster signal 421 is provided and the imagnitude of fits frequency relation signal 400 is lies thin the steepshots of pulse within modulation signal 415. againtic of the trought years again we use given the pulse width modulation sign for wards, such up discuit 410 will illow the sweeter as long as soft salest emitte signed in his gaptach of the pulse width modulation of the pulse with modulation of the pulse with modulation signed in Fig. 4: in this way, the insush cross picted in Fig. 4: in this way, the insush p

ion of soft stant circuit, 410 will at

### 6,107,851,

Refuring to PIG. 5, frequency variation signal 400 when is prostedly professed to have a constant period in provided to the main excitator of the provided to the main excitator 465. The conguisted of the patter width modellater correct 615 will approximately be the magnitude of feedurery variation signal 400 divided by the spinstance of testians 750 place the magnitude of the correct general source 470. In this way the pulse width modelator current 615 will vary with the magnitude of the frequency variation signal 400. The result is that the frequency of probability signal 50 varied according to the magnitude of the coursed. It is presently preferred that the pulse width modelator carrent states produces a constant current. width anothing course and to protect a constant current having a megalinde of reclay polast ane (12.1) amonampeure, and that the purpose written signal induced current \$27 varies between zone (0) and cight landwed (2010) refull the Edd generated by the power supply

processes as a consequency me power apper ages FIG. 6, so returness presently preferred pales defined switch 262 londades all of the same char-ic described with respect to FIG. 3. In addition to appearate, a scientific frequency variation circula mace, 562 and transinos 655 are added to the variation circuit 403. Texnistry 655 in activated

dieds. 768 in order to moletajn a contingues-with toal 720 yildish has a facultonic circuit coupled in contingual personal printerpol lecthock check magneties an opin 800 and super dieds 520. The neutral 625 of regulation is coupled to the facultonic terminal 825 of regulation circuit 830a on any off at a driverych that is constant at a given in the continual state of the continual sta

circul 200 when the regulation circul 200 km in the open of the power supply will now be described. Operation of the power supply will now be described. AC mains value is known from the two the continuous continuous values is input through EMI films 700 into but excition 710 which provides a rectified signal to possibly expections 220 that provide input DC voltage 725, allows case they primary winking 740 the primary and should coast obly operates at a given input DC voltage 725, allows case to the MI though primary but and post of the SMI through primary winking it was the cash to the MI through primary winking. 740 the state of the MI through primary winking 740 in the state of the MI through primary winking 740 in the state of the MI through primary winking 740 in account with find the control of the MI through 750 in the state of the manufacture 730 is defined as exceeded with the control of the manufacture 750 in the first power to the kind 730. The voltage cases also 770 with 770 will your through the control of the money detecting a first power to the kind 730. The voltage cases also first power to the kind 730. The voltage cases also first power to the kind 730. The voltage cases also first power to the kind 730. The voltage cases also first power to the kind 730. The voltage cases also first power to the kind 730. The voltage cases also first power to the kind 730. The voltage cases also the case for the money of the account when the 730 will be not the first power to the kind 730. The voltage cases also the first power to the kind 730. The voltage cases also the case for the case of the account when the first power to the kind 730.

manuscrat is a constant level.

It is presently preferred that the au-cross opineougles 800 and the sever of sear clock 820 is approximately heatfold level, When the voltage waters the deschold level, correct it oppose capacity is a constant of the constant

Although the personally performed gower compaly of PIO. If nilities chareot monte regulation and a feedback circuit that includes an optocomplex and a sear-finding, the pursues investigation of exploration and assert finding, the pursues investigation to the option of the present investigation such a feedback; no method to electric littles content or voltage monte regulation may be utilized by the present investion without departing from the spirit and suope of the present investion so long as a signal indicative of the power suspicied to the feedback remaind IES of the regulation 25 circuit ISO. Additionally, although the present investion 25 circuit ISO. Additionally, although the present protection of the feedback circuits before feedback circuits protected as part of feedback circuits before feedback circuits may be militarely by the present investion without departing from the spirit and acope of the present investion.

Regulation circuit 450 also such have integrated and sent coupling of the couple its switched on, a power up signal is generated within; the intensal circuits (or regulations circuit SiO. A power up signal is used to tagger soft start circuitry that reduces the thry circle of the switch that operates within the pulse middleton departs of presently preferred for by an (10) milliconnect, Opera and start operation in the complete, regular day operation in the complete day ope

cycle.

Alternatively, or is addition to soft start functionality, regulation circuit 838 may step have Requesty filter functionality, regulation circuit 838 may step have Requesty filter functionality. That is, the availating frequency of the regulation circuit 838 varies seconding to no interapt frequency varieties, and the signal. This has an advantage over the funquency filter operation of FIG. 1 in that the frequency maps of the pursuantly explained extends 838 is become and fined, and is put subject to the line voltage or lead magnified; varieties.

Referring to FIG. 9, frequency varieties circuit 445 and note considerer 443 function or head of the best of the varieties. The report of the bright and low that of succliman day cycle algorithm circuit 818 A. At secondly preferred regulation circuit 818 and in standy-state pertains in depicted and described to expanding potent polication face. No. 60012, 520 which is hereby incorposed by references in its entirety.

The regulation circuit FIG. 9 can be modified in fact-the tomage carms assume.

and regulation circuit of FIG. 9 can be modified to include an a second current source to flusher increase the period of small nordification signal 415 which achieves the same result and firmation are described with respect of FIGS. 6, and 7.

The soft start functionality of the parametry preferred regulation circuit 200 of FIG. 9, well shorten the on-time of an armited 430 to ham due to the samples of the switch 430 to ham due to the sine of the nantiquent deep-cycle signal 607 as long as she soft start combit signal 421 in

topis possible without deviating from the spirit of the inventive croccepts described herein. Thus, the invention are not to be austrated to the performed embodiment, specification or playings. The protection to be afforded this patent should threshow only be assisted in accordance with the spirit and intended scope of the following claims. What is claimed in:

1. A paine width modulated porisch comprising:

- a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said motion terminal according to a drive signal provided at said control input;
- verseem ngene; an excilient the projekte an exciliation rignal having a inspensey range, said frequency of said, exciliation signal varying which raid frequency range accounting to said frequency variation signal, and oscillator fredier providing a necommen skyl cycle signal comprising a first state and a account state; and

- providing a nacissum diety cycle signal comprising a feet suit and a second shale and a derive signal when suit nectume due ty cycle signal is in mid flest state and a unagabatic of said occiliation signal is believe a synichte threshold level.

  2. This judge width modulated points of chim I whence said first states, and a state said first states, and a state said first states, and frequency variation circuit comprises an activities and coefficient, and frequency variation signal in said occiliator, and frequency of said occiliators signal warring within said frequency represents variation signal.

  4. The pulse width modulated switch of chim I further comprising a soft-state circuit that provides a signal featuring said drive circuit of discussions signal as a superior when said unagabated of said frequency variation signal.

  5. The pulse width modulated switch of chim 4 wherein and sufficient designal provides a said state signal when said said state signal soft state state to said soft state signal.

  6. The pulse width modulated circuit of chim 4 wherein and additional statistic speaks a comparator saig seconds.

  8. The pulse width modulated circuit of chim 5 wherein said additional statistics of safety of chim 2 wherein and additional statistics of safety of chim 2 wherein and additional statistics of safety of chim 2 comparator safe provides a comparator singulation of control or comparator safety seconds.

on lovester that sectives said or provides said soft start signal. 7. The pains width modelsted said

10. The pulse width modulated switch of claim 2 whereis id variable phesisheld level is a function of a feedback and received at a feedback terminal of said polse width

- 13. The angulation crows a single instruc-a such start clients that provides a signal instruc-tion to discontinue said drive signal accor-abilities of said figuraccy variation signal. 14. The regulation circuit provides a soft a transcorp variation circuit provides a soft a valuation said and start circuit crosses open and its acmoved.

- a conjugated file provides a comparable signal when a magnitude of a effection signal is greater these or equal to a energitude of said frequency varieties signal, and as investor that specifies and comparator signal and-provides said soft man signal.

  16. The engulation closest of claim 11 whereis said first terminal, said second terminal, and switch, said frequency, varieties eiterit, and said drive classic comprise a mono-fetic desire.

# PX3

(12) United States Patent Balakirshnan et al.

US 6,229,366 B1 (10) Patent No.: (45) Date of Patent: May 8, 2001

- (54) OFF-LINE CONVENERS WITH INTEGRATED SOFTSTART AND PREQUENCY SITES
- St. Bulle Ballalderhauer; Alex Bjeuguerha both of Susange; Luff Lund, Sur Jusa, all of CA (US)
- CA (US)
- Subject to any electrimes, the ter patent is extended or adjusted t U.S.C. 154(b) by 0 days.
- (21) Appl No.: 99/573,981
- (22) Filed: May 16, 2000

### Related U.S. Application Data

- (62) Division of application No. 89/080,774, filed on May 10, 1996, new Feb. No. 6,197,831.
- (SI) Int. CL7 ... 1103K 3/017
- . **337/1712; 32**7/14**3; 327/53**3; 337/544
- de Sparch 327742, 143, 327742, 143, 327742, 143, 327742, 176, 176, 176, 176, 176, 596, 531; 544
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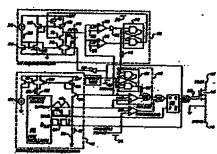
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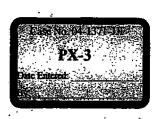
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crive rigual when the maximum duty cycle me first state and a magnitude of the oscillation sig-a variable threshold level.

18 Chilos, 9 Drawing Sheets





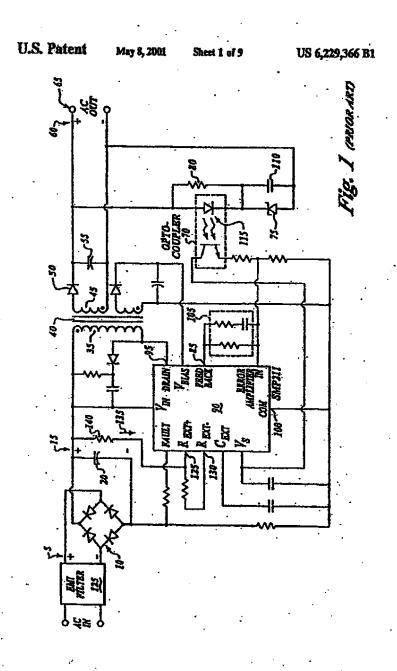
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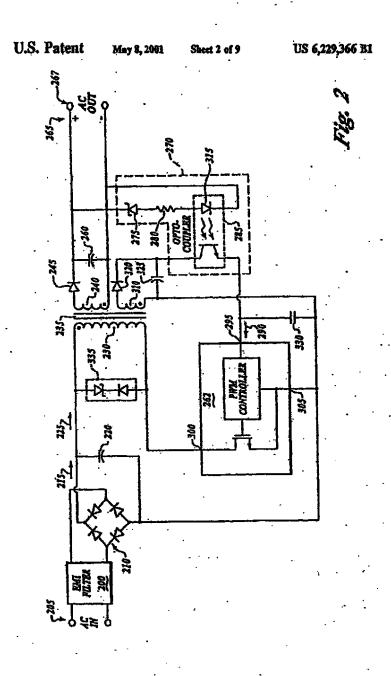
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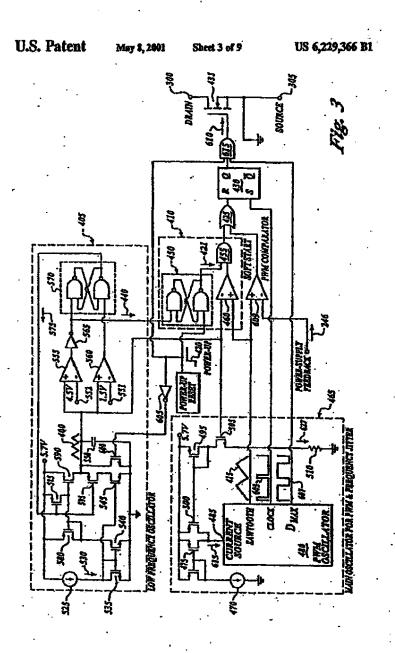
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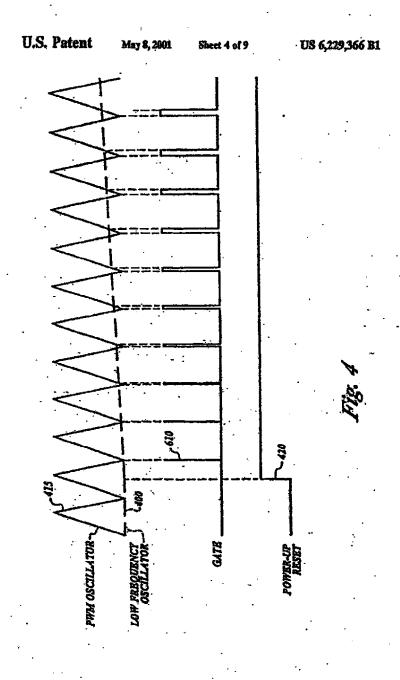
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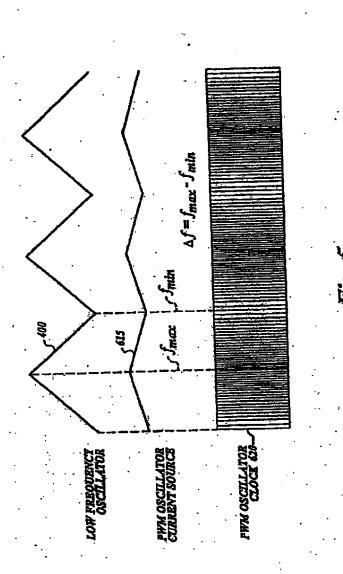
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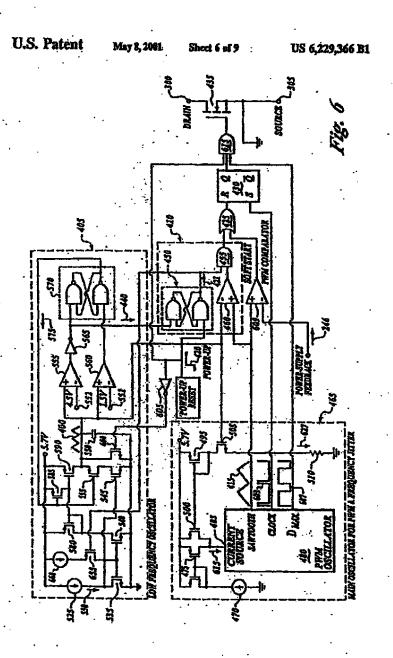


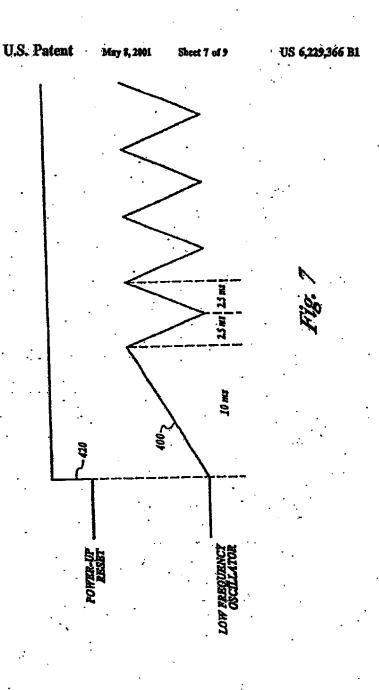


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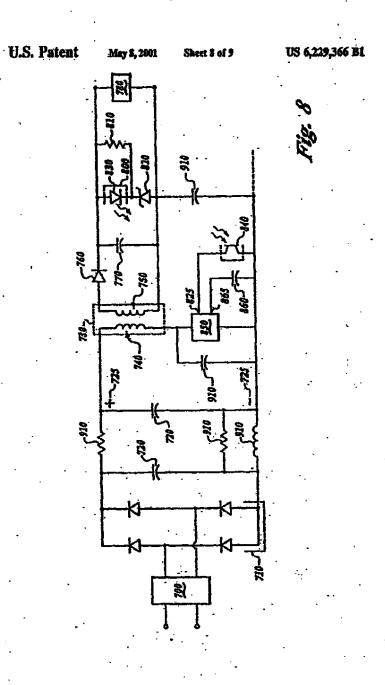
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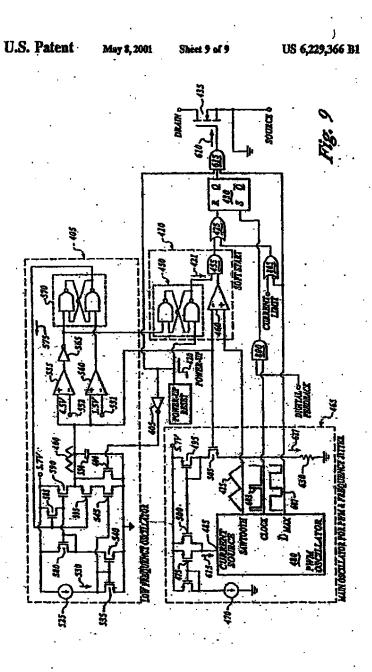




PIF 00225



PIF 00226



# OFF-LDIE CONVERTER WITH Dytegrated Soptstart and

## CROSS-REFERENCE TO RELATED APPLICATION

This is a Divisional of U.S. application See. No. 89080, 774, Sleel May 18, 1998, now U.S. Pat. No. 6,187,851.

# BACKEROUND

# L. Field of the lovestion

The field of the present invention pertains to the field of over supplies and smoog other things to the regulation of

applies that convert as AC as Power suppose an accuracy and a checkmaic devices, amongstokes devices, are known. The power supplies are required stain the colput voltage, consent or power within of range for efficient and safe operation of the ple registant range for caseman and and appearing a point width modulated control to unionist the onlyst voltage, casem, or power of the power supply within a regulated range are also known. These switches makes an excellence and related

power of the power supply white a regulated page are also known. These switches utilize an entitleter and robated circulary to vary the evolution frequency of operation of the switch, and therefore supplated the power, current or voltage that is supplied by the power supply:

A poshious with utilizing pulses withit succludated awitches is that they operate at a scholarly high frequency companed to the frequency of the AC mains voltage, which results in a high frequency signal being generated by the power supply. This high frequency signals is injected back into the requency signals are the medical by the power supply. This high frequency signals are the medical by the power supply as advertagementation wases. These high frequency signals and in the Electromagnetic hierafracture (EMI), of the power supply, and in their are the largest compliants to the EMI of this power supply. The EMI generated by the power supply, and in their are the largest compliants to the EMI of this power supply. The EMI generated by the power signals which theremes a component of the AC mains signal with the provided to other devices for the power gript which also causes notes problems for those devices. Farther, the resisted EMI by the power upply can interface with mode and televished to extend these three means and over the air by various entitles.

To combast the problem of EMI, acrossil gracultarious

transmitted over the sir by various cultifies. To combut the problem of Edd, several specifications have been developed by the Federal Communications Committee (FCC) in the United Strate sail the Beneficial Community (EC) have catabilished aphellication that specify the maximum resount of Edd that can be preduced by cleaner of electrosist devices. Since power supplies generate a major component of the Edd for electronic devices, an ast important steps in descipating a power supply is lovely with the acceptable limits of the values simplests. Since, a power supply to the utilized to many different connectes of the would, the Edd power supply to the utilized to many different connectes of the would, the Edd power supply can be utilized to many different connectes of the would, the Edd powered should be within the court efficiency of limits wouldwide to allow for maximum stillimiton of the power supply.

A hance way of minimizing the EMI provided by the power supply in by adding so EMI filter to the imput of the power supply. An EMI filter generally utilizes at heat one inductor, capacitar and resister in combination. However, er EMI produced by the power supply the larger the

conspicuous that are talkized as part of the IME is cost of the IME there is in large past determined by of the laductor and expection unified. The loc components, the higher the cost of the gover Purtler, simply utilizing as EMI filter decirated and radiated EMI.

Another problem associated with pulse wrom memorial whiches results from operation of the power supply at start whiches results from operation of the power at the onlyst ip. At stars up, the vol power supply will essentially bred switch will then condu sible account of time in each sycle of opera sible account of time in each cycle of operation. The scale of this is a maximum insuch current into the power supply. The association forms from the control is greater then the current that is utilized thating normal operation of the pursus supply. The maximum insuch current streams the components of power supply and switch. Stress is specifically a problem for the switch, or transformer of the power supply. The switch, or transformer of the power supply, and the monutary side components of the power supply and the switch decreases the overall life of the power supply and increases the cost of the power supply because the nucleus rating of the components used in the power supply to an destinct from the insule currents will be greater than the maximum rating required for consul operation.

required for corneal operation.

Further, when the pulse width modelated switch conducts for the maximum possible amount of these in each optic of treatment apply its maximum possible amount of the least optic of the power supply often does not imputed as fast as the secretary frequency of the reside, the rapid these of the voltage, current and power will often result in an overshoot of the sections with the regulation range which will cause though the device being supplied power by the power upply.

Returning to Will 1s toward amount on the sections.

Returning to FIG. 1.a known gover supply that at to all minimum EMI and reduce statusy steem is highly section 10 reculing the filtered AC analys voltage 5

to affinishe EMI and reduce stating stees is depleted. A section 18 rectifies the filtered AC ensign veilings 5, from 184 filter 120, input by the AC insigns by generate a restified voltage 120, input by the AC insigns in generate a substantially DC voltage with a signal configurant. This restlict voltage 15 with sipple component in previded to the principle voltage 3 of transformer 40 that is used to provide power to accordary winding 45 of transformer 40 that is used to provide power to accordary produced to accordary provides 30 and accordary conjuctor 55 that provide a accordary DC-voltage 40 at the power supply output 63 to the device that is complete to the grower supply.

In order to maintain the accordary DC poltage within a pupulate samp a facilities from the power supply.

In order to maintain the accordary DC poltage within a pupulate plate 35 of pulse within nondiluted which 95. The voltage stagnated control of the power supply of the power supply of the power accordance in the desire terminal 25 and commands benefit and the power supplied to the power within have controlled another by 184 to the power within the power within the principle of the power supply owjest 65 is have which in prover supplied to the power supply owjest 65 is have which in the facilitate power to open the own of the power within the facilitate power to open the control that output to the forther to the control of the power of open to of the power within the facilitate to accordance in the facilitation of the power within the facilitation of the power within the facilitation of the power accordance of open to other the total which of the facilitation of the power within the facilitation of the power accordance of the po

formula convents are minimized at start up by one of soft start capacitor 110. Soft start interfaceshy in agence to be a functionality that endoces the fareth currents at start up. At

extent a coursel begins to flow through foodback or 30 and thereby into sell stirt especier 11%. As the ps of soft stast capacitor 11% increases slowly, comme ast not asset capacities LIV increases storely, commit we though light smithing dicho ILS of quicocopies 70 constraining the duty cycle of the stylich. Once the of the not stast capacitor ILV suches the towers more values of account liche 72 cursus will flow resear diods 75. The approach described shows will through zener dinds 75. The approach described shows will, nothout the humbe currents into the power supply, however, it will be noverall cycles before the light emitting shock 115 will be glo conducting. During the several cycles the tension mirrals causest will still flow through the primary winding and other accordary side compounds. During these cycles the transformer may patents, and therefore the interfere the interference may have no be designed withing a higher one sentence was a transformer may be higher ones at higher ones and the area of ooft start expection as in FIG. 1.

To reduce the TEMI counts by the names attention on PAII

man would be required for somma speciation with the same of soft shat capacition as in FiG. 1.

The reduce the EMI output by the power supply an EMI filter 120 is wilload. Additionally, pulse within nordalised switch 30 is equipped with frequency confination terminal 1225 and 136. Frequency oscillation terminal 1225 and 136 receive spilar coursed 135 that varies according to the apple component of substantially DC voltage 23. The filter current 135 is used to vary the frequency of the anni-inother 135 is used to vary the frequency of the anni-inother 135 is used to vary the frequency of the anni-inother 135 with modulated awhich 50. The new toolsed waveform generated by the conflictor is compared to the freedenic provided at the foodback pass 28. As the firequency of the switch complete between the standards represent of the switch to be spread over a larger bendwitht, which minimizes the post-tubes of the EMI generated by the jover apoply at each frequency. By endexing the EMI the ability to comply with precument standards in increased, because the government standards in increased, because the government standards would not all the special of the amiliation of the patter with annihilated evolute of the special of the continuous formation of the patter with socialisted evolute by varying the seculistics frequency flows. A problem apposituated which the EMI reduction scheme

inquemey of the oscillator is inferred to us Sequency jitter.

A perihem speciated with the EMI reduction urbanedescribed with respect to FMS. In this this pipe component
will have variances due to varieties in the fine youther and
output load. Additionally, also in the high test may vary, design
and the component value of EMI resister 140 is difficult to
determine and oncerpositingly design of the power supply
becomes problematic.

# SUMMARY OF THE INVENTION

In one embediment the present invention comprises a white width modulated awards comprising a switch that flower adjust to the transmitted between a first terminal and a second tentional according to a drive signal. The pulse width modulated awards also comprises a frequency variewhich mechanised switch also completes a frequency varia-ities check that provides a frequency variation signal and as as-necifiator that provides as excitation signal having, a for-quency fast venies within a frequency range according to the frequency variation signal. The carditator further provides a maximum duty cycle signal completing a first astar and a account size. The pulse with anotherised circuit further as-comprises a drive circuit that provides the drive signal when the inactions duty cycle signal is in the flex tasts and a magnitude of the oscillation signal in below a Variable a—A-chil lend.

Another enhadiment of the person invention comprises pulse width modulated switch comprising a switch con-ising a control input, the switch allowing a rigual to be

ecoding to a drive right. The price w swhich also comprises an oscillator that provides a measurem duty cycle signal comprising an one-take said as off-cities, a drive special start provides the drive signal, and a soft start circuit that provides a signal instructing said drive circuit to disable the drive signal desires at least a postion of said co-state of the maximum day optic.

on-mass of the maximum duty optic.

In an absence embediment the present invention compiles a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal, a drive circuit that provides the drive signal and a not start circuit that provides a signal instructing the drive circuit to disable the drive signal.

le yet austice embedience the persent investion com-prises a regulation circuit comprising a switch that allows a signal to be reasonabled between a first temperary variation formed according to a drive signal, a lenguescy variation circuit that provides a frequency variation regard, and advive circuit that provides a frequency variation are made and advive circuit that provides a drive signal for a sacricum lines period of a time druttine cycle. The time detailon of lic-cycle varies according to the frequency variation signal. In the shower referenced cashe-dimense, the pulse width modulated switch or regulation circuit may comprise a monalistic device.

An ebject of an aspect of the present invention is directed a yelso width modelship awaich that has integrated soft

start espainifies. Another object of an aspect of the present investion is directed towerd a point width modulated switch first has integrated frequency variation capabilities.

Yet unplies object of an aspect of the present investion is directed towerd a pather width modulated switch that has integrated frequency variation capabilities and integrated soft start capabilities.

A further object of

A further object of so sepect of the per

An enter copies at an appet to the greates inventors and freezed breat and frequency variation emphyliates.

This and other abjects and appets of the person inventors to the period, depicted and described in the dynamics and the description of the inventors contained breats.

# BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a known power copply stilling a pains width modulated switch, and statemed soft start, and dropously jitter functionality. FIG. 2 is a personity preferred power copply stilling an pains width modulated switch according to the present invention.

PRIC. 3 is a presently preferred pulse width mod which according to the present invention, FRIC. 4 is a leading disposes of the multistant operation presently performed pulse width modulated awritch according to the present invention.

persondly perfected pulse width modulated switch according to the present feveration.

FIG. 3 is a tituding diagram of the frequency jates option of the personally preferred poles width modulated on according to the present invention.

FIG. 6 is an absence presently perfected pulse to modulated switch according to the present invention.

FIG. 7 is a liming diagram of the optionsis of the absence of the present presently preferred pulse width modulated switch of Fig. 2 is a presently preferred power supply withful regulation executing to the present invention.

RG.9isay

# DESCRIPTION OF THE PREFERRED

Referring to FIG. 2, BMI litter 260 is compled to an AC nation voltage 263. The AC mation voltage 263 is needled by occiding 124 is a powified to power supply capacities 226 which provides a substantially DC voltage 273 is powified to DC voltage 273 is powified to DC voltage 273 is provided to DC voltage 273 is provided to the primary winding 270 of transferring 233 which store in savingy provided in the primary winding 234 is no longer receiving nearry, energy is delivered by the transferred 250 to the secondary winding 240. The voltage induced across the according winding 240 is rectified by sectified 245 and then transferred into according to the primary winding 240 and provided to the power supply object 267.

Theory is no longer provided to the primary winding 234 when the pulse width modulated switch 252, which is 26 coupled to the primary winding 234 on the primary winding 234.

when my pure worse monutes review as, where is coupled to the primary winding 230, course conduction. Pulse width modelated spring 2CC is a switch that is controlled by a pulse width modelated signal, Pulse width modelated style. These width modelated style of the width modelated spring. Pulse width modelated spring. The conduction and ceases construction. modulated switch 262 conducts and crases conduction according to a duty cycle, that it is just determined by fordinct from the power supply output 267. Paths with modulated switch 262 is a switch that operates according to prine width modulated accomplished to this poles width modulated switch 262 is a switch that operates according to prine width modulated according to produce the switch 262 is a scenario to the print 200 and operately 267. Which is presently perfect to compute a most close 275 in series with a maintar 200 and operately or 263. Opiniospies 265 provides a fordback current 250 to flooblack terminal 250 of pube width modulated switch 262. The fordback current 250 to flooblack terminal 250 of pube width moduly cycle of a switch cought detwoerthe first terminal 360 and social terminal 365 and first angulate the output vollage, current or power of the power supply. shigt, contest or power of the power supply.

Although, it is personly preferred that the conjust voltage is tillized for factback, the present lovestient is also capable of utilizing either the content or power at the power copyly output 267 without departing from the spirit sedecage of this

A portion of the current ampelled as the feetbeck terminal:

25 is utilized to supply bits power for operation of the
pulse width mediated switch 262. The constanter of the
current logut at the feetback terminal 283 is utilized to
current the duty cycle of the pulse with modeland aspira262, with the duty cycle of the pulse with modeland aspira262, with the duty cycle being invessely propositional to the
featback current.

izativel: carrent.

A blue valuding 310 in utilized to bine opinocopier 283 so that a feedback corrent can flow when light enduding diode. 313 of opinocopier 283 canducis. The power supplied by the bine valuding 310 is also used to charge palet width acodelation capacitat 330, the energy from which is willined to power the pulse width modelated switch 262.

Overrollage protoction circuit 333 is utilized to prevent overvoltages from propagating through to the transformer 233.

e commonly council opted became by sel No. 5,014,176 which is incorp

transical 205 are the electrical input moder pulpet p the point width modelated switch 262. They need no

shillifes. When the device to wi stat capitalities. When we were a power up supply is coupled in switched on, a power up a security of pulse with the interest circuity of pulse with the control of the con lated a which 261. The power up sign stant clausely that reduces the duty cycle of the switch that operates with its the pates with modulated switch 242 for a producerulined period of time, which is presently preferred to be ten (109) milliocroads. Once soil sized opionition is completed, joiles width modulated awards 243 operation in completed, joiles width modulated awards 243 operates according to its regular deep cycle.

Altomatively, or in addition to soft start functionality,

Attensatively, or in artificies to soft start functionality, paths width modulated switch 267 may also keys frequency just functionality. That is, the switching funguency of the pates width anotheled switch 262 varies according to instantal frequency variation signal. This has an advantage over the frequency just operation of FIG. I is that the frequency range of the personally perfected paths width modulated switch 262 is known and fund, and is not subject to the Nam woltness or look magnitude variations. At low monuments avenue to move an inner, and is yet angue to the line voltage or lood megatistic variations. At low powers, those less than approximately ten (10) wetts, the common mode choice which is often utilized as part of the [240 Sher 126 can be replaced with inductors or missians.

As can be seen when comparing the power supply of FIG. 3 to first of FIG. 2 the number of components willing in reduced. This induces the circuit cost of the power supply so well as inducing its size.

es well as nothering its size.

Refearing to Fife, 3, frequency variation signal 400 is sufficient by the pulse, with modulated switch 262 to vary its switching frequency within a frequency range. The finquency variation signal 400 is provided by frequency variation signal 400 is provided by frequency variation of real 405, which preferrably comprises me oscillator that openhes at a lower frequency than main oscillator 465. The frequency variation signal 400, is presently preferred to be a triangular wavefrom their preferrably oscillates between the results frequency variation signal 400 is a triangular waveform, alternate frequency variation signal 400 is a triangular waveform, alternate frequency variation signal status status is that as terms signals, consist output signals are offer variation rigual vev ... and south 263 to very its signals areas around a supports, consists outlier of greats are offer signals that vary in reagaineds during a fixed period of time may be utilized as the frequency variation signal.

intry the utilized as the favguency variation signal.

The frequency variation signal 400 is provided to acit
sitest sircuit 430. During operation and state circuit 430 is
also provided with pulse, with accountation frequency, signal,
435 and power up signal 426, 800 start enable signal 425
goes high at power up and remains high util considerer
signal 400 reaches he peak value for the first time, Soft start
circuit 430 will provide a signal to or-gate 425 to react state
438 thenthy descripting conduction by the index 435,
which is presently preferred to be an MOSFET. Soft start
circuit 41th will instruct switch 435 to cause conduction
when the circuit must easily since 435 to cause conduction circuit Alth will fusionst switch 435 to cause conduction when the soft start enable signal 421 is provided and the magnitude of the frequency verteines signal 400 is less than the magnitude of poster width modulation algost 435. In order words, attest up circuit 430-will allow the switch 435 is conduct as long as soft start enable signal in high and the megatitude of the pulse width modulation signal 415 is below the semplester of frequency varieties signal 415 is depicted in FIG. 4. In this way, the insula comment a strateg-will be finaled for all cycles of operation, feelbeling the first

The pulse width modulated switch 262 depicted in FiG. 3 also has frequency jiller functionality to help reduce the 25th 1 generated by the power supply and poles width anothering switch 262. Operation of the frequency jilter functionality will now be explained. Make obtained 455 has a terrent will now be explained. Main excitator 445 has a current source 470 that is miscoust by scitter current source 470. Main is miscoust by science current source 470. Main cocidator drive corrent 515 is provided to the current source input 485 of PWM oxiditator 480. The magnitude of the current stops into current counce; huge-485 of PWM oxiditation signal 415 which is provided by PWM oxiditation curlitation signal 415 which is provided by PWM oxiditation 480. It needs to very the frequency of the public width smoduleties oxiditation signal 415, we additional time width smoduleties oxiditation signal 415, we additional current current source 460. The acilhteir 480. In order to vary the finguistry of pulse and above co-liberon signal 415, we additional cur-ness 495 fit, provided within teads spelitheir 465. The sal, estreat source 495 in subsocial by additional sources source 595. The correct provided by addi-ments source 495 is whipe as follows. Proposacy on signal 400 is provided to the gate of souls oscillator or 395. As the singuished of finguistry variations MO increases so does the voltige at the source of military and the source of the contractions of the contractions.

in fed felo first transister 540 and fed july third to 100 organi 400 is greated a remeracy serv cispectorics, warms altered for a measurable city in one embodizated of the pulse width mechanical services. This frequency variation signal 400 is provided as aspect final comparative. 353 and lower final comparative 353 and lower final comparative 353 and lower final comparative 354 and lower final services. The high when the magnitude of the frequency variation agout 400 careods the expect threshold voltage 352 which is presently preferred to be four print five (1.5) while, it presently preferred to be from print five (1.5) while, it presently preferred to be one point five voltage 357 which is presently preferred to be one point five voltage 357 which is presently preferred to be one point five voltage 357 which is presently preferred to be one point five voltage 357 which is presently preferred to be one point five voltage 357 which is presently preferred to be one point five voltage 357 which is presently preferred to be one point five voltage 357 provided to the frequency variation circuit invest first comparator 358 he operation, the operation of frequency variation signal 400 were final to comparator 358 will be made and the street freedold 357, 1.5 while, the operation signal 400 more final to comparator 358 will be seen paid of the majority of each cryst of frequency variation signal 400 more final to comparator 357 will be made as a proper final to comparator 357 will be not provided to the result freedold 357, 3,7 while, and the lower final to comparator 358. The output of upper limit is made as the result is put will be majorited of frequency variation signal 400 cache cryst of the species of which the street is put will receive a high signal soft final signal 352. This impacts the street is put will receive a high signal soft final signal 352 will be subject to the street final signal 352 will be subject from circuit capacity variation signal 400 exceeds the uppear variation signal 400 exceeds the uppear variation signal 400 exceeds the uppear variation signal 400 exceeds the uppe

its first cycle of operation.

Study citel a specificat of the pulse width modulated pointh 202, in, non earn up operation, will now be described. FWM oscillator 600 provides pulse width modulation institution signal 415 to pulse width modulation comparator 600, the output of which will be high when the magnitude of pulse width modulation signal 415 to general rand to magnitude of a feedback signal 294 which is a feedback see magnitude of a feedback signal 294 which is a feedback see output of pulse width modulation comparator 600 is high a sign 425 in tiggree to up thigh, which in term reacts pulse width modulation latch 430, accessing the an aignal from the control input switch 435, thereby tensing of

no occamient was a med-gate, receives the standard of the standard of the standard of clocks signal 607. As long as each clock signal 619 is provided to the publish is complet between first of templat 305 of the pulse width unts Jow and section terminal 200 of the jungs white halded sowhith 262. When any of the output of pulse th modelstine high 430, power up algori 424, or mari-q dary cycle signal 407, goes low kinys signal 610 is on per provided and switch 435 occurs conduction.

longer provided and switch 435 ceases conductive.

Referring to FfC. 4, frequency variation signal 480 preferring to FfC. 4, frequency variation signal 480 preferring than a period, which is greater than the of pulse with nordative occiliation signal 483. The yearsely perfected period for frequency variation signal 480 is treasty (20) milliseconds, in ordat to allow for a smooth stat up period which is sufficiently longer than the period of pulse width succellated signal 420 which is presently perfected to be ten (20) unforced. Device signal 480 will be provided, only when the magnitude of pulse width modulated signal 415 is less than the magnitude of pulse width modulated signal 415 is less than the magnitude of pulse width modulated signal 415 is less than the magnitude of pulse width modulated signal 415 is less than the magnitude of pulse width modulated signal 415 is less than the magnitude of pulse width modulated signal 415 is 200 will be prefetably indicated charling from low voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the magnitude of pulse voltage when power up algoring the first than the pulse of the p

Further, frequency vertained signal 400 will be preferably instituted stricing from low voltage when power up along an 400 in provided.

Referring in PRL 5, frequency variation signal 400 which is presently preferance to have a constant period is provided to the main energhine 465. The magnitude of the pulse width modulator catenats fills will approximately be the magnitude of frequency variation signal 400 diploid by the maintaines of sections 250 place the magnitude of the crosses produced by current source 47th. In this way the pulse width modulator catenat 615 will very with the magnitude of the frequency variationalized 400. The recent is into the frequency of pulse variationalized 400. The recent is into the frequency of pulse variationalized 400. The recent is into the integratory of pulse variationalized 400. The recent is into the integratory of pulse variationalized 400. The recent is into the integratory of pulse variationalized 400. The recent for pulse with modulation signal in variation signal induced on the state of the pulse variation of the state of pulse of the pulse pulse pulse and the grantified with repeated pulse within modulation outilized 400 and toward for the pulse pulse for the pulse pulse in the grantified by the power supply.

Referring to FRL 5, an allocated pulse worms inagnitude and the grantified is all frequency leading within the company inagnitude and the grantified by the power supply.

Referring to FRL 5, an allocated pulse worms inagnitude with the A00 gas income of the pulse of the first pulse of the decreased eyein justiced will fasther decrease the green peak levels of the EME give to specifying less that at each fac-

445 will preferably have a period of ten (10) mill its first half cycle. After that, when the trees larged on the period is professably decreased

militarounds. Palse width modulated switch 262 is presently
preferred to be a neutrilitie device.

Reluting to 1916, 2, a power amply comprises a bridge
rectifier 718 that rectifies an impet AC mains voltage. Power
supply capacitors 720 therips with the excitied AC mains
voltage to maintain as input DC voltage 725. Is approximately
go rectifier 718 that rectifies an impet DC voltage 725. Is approximately
to maintain display for input DC voltage 725. Is approximately
to rendered complete for input DC voltage 725. Is approximately
to rectified AC saids and the foreign the control
to state the said of the power by the composition of the power supply also
includes beamonic filter temposates 910 which in considerable and the power grid. Passelment 730 includes
a primary winding 750 magnetically coupled to accordary
winding 750. The secondary winding 750 is compled to a
diote 760 that is designed to pervent current frow in the
secondary winding 750 when the regulation circuit 850 is
econducing (an estate). A capacitor T70 is compled to 14.

25 precently performed feedback clicait complete to 14.
26 precently performed regulation circuit 850 and capacitode 150. The output of approximate in

27 things 740. A regulation circuit 250 orticines
also and off at a duty cycle that it constant at a given input DC

28 voltage 740. A regulation circuit 250 witches an and off at a duty cycle that it constant at a given input DC

29 voltage 740. A regulation circuit 250 is in the am-time.

29 printing Of the power supply will now be described. As

20 printing of the power supply will now be described. AG

20 printing voltage is broth thrown 2504 for 160 to take a

especitor \$60 is complete in and anogetics power to regulation circuit \$50 when the regulation circuit \$50 is in the con-table. Operation of the power ampily will now be described. As AC mains voltage is input through EMI Site: 700 is to bridge at recitive. The widels provides a recitive of the winds provides a poster supply especies 700. He specifies of the Site powers apply especies 700. He specifies a figure 100 voltage 725 is primary winding 740. Regulation circuit \$50, which poster poly operates at a question frequency and shoot constant duty cycle at a given input DC voltage 725. Ultuwa current as to store through primary winding 740 during its on state of each switching cycle and sets as open circuit in its off size. When current from friends primary winding 740 content in its off size. When current from friends primary winding 740 examples former 736 is attoring energy, when to custout its flowing forces 736 is attoring energy, when to custout its flowing any winding 750 dues provided the currenty to exploite 770. Capacitor 778 delivers power in the load 780. The voltage across the load 720 will vary depending on the smooth of energy stored in the transformer 730 is account in the load 780. The voltage create the load 780 is allow the voltage delivered to the load to be 50 maintained at a constant level.

It is presently preferred that the most of the widing drop account protection that the most of the widing drop account protection of the voltage drop account protection of the contract that is a firme account of the widing drop account protection of the contract to the side of the maintained at a constant level.

It is presently preferred that the most of the widing drop account protection of the side of the protection of the widing drop account protection of the side of the protection of the side of the second of the second of the side of the second of the side of the secon

mainteined at a countest level.

It is presently preferred that the save of the voltage drop across ophosospies 1900 and the revenue break down voltage of green diode \$30 is appreciately equal to the desired developed level, When the voltage across the lead? 70 reaches the flushfull level, causest beight to flow thiospit the uptoroughle 900 and enter their \$20 that is sure is used in disable the regulation clocak \$30. Whenever regulation clocak \$20 is in the off-case the regulation clocak power apply hypers capacity \$60 is chalged to the operating tophy voltage, which is presently postered to be free point server (\$7.7) volta by allowing a small current to flow from hypers tempical \$65 to the regulation clocak power supply

was activized to according to suggistion elevation repulses gover to the load 780. Once the remaining tracey in transformer 750 is delivered to the load 780 with the voltage of the load 780 will decrease. When the voltage at the load 780 will decrease. When the voltage at the load 780 decreases below the traceful load, control cases to flow through opiniousles 780 and regulation circuit 850 resumes operation either instantaneously or nearly instantaneously.

circult 839 resumest-operation either instantaneously or usually instantaneously.

The presently preferred regulation circuit 830 has a correct limit feature. The current limit have off the segulation circuit 850, when the current flowing through the segulation circuit 850 these shows a current streated level. In this way regulation extend 850 can reset quickly to changes such as AC ripple that occur in the restitude AC mexics writing, and AC repute the constant in the restitude AC mexics writing, and helicon from the propagation of the woltage changes in the land. The current limit increases the responsiveness of the regulation circuit to input voltage, changes and delivers constant power cusput independent for the AC mexics input voltage. Although the presently preferred power supply of FIC. 3 millions current mode segulation and a factback change the includes a correct mode segulation and a factback change there.

Although the presently preferred gower supply of FIC. 2 milities convert mode regulation and a faceback clearly that includes an optococycles and senter dialet, the present levention is not to be construed as to be fainfied to such a faceback clearly the method or clearly. Ether covered or values much supplied much or spirit and accept of the present frequenties along a signal indicative of the gower supplied to the load is reputed to the though the supplied to the faceback transless RCS of the reputation power supplied to the though the supplied to the faceback transless RCS of the reputation power supplies both utilize an exploringly and sense disks as part of faceback circuits show the faceback circuits and stops of the present invention.

Regulation circuit RSS also may have integrated and stop spirit and accept of the present invention.

Regulation circuit RSS also may have integrated and stop to coupled its switched on, a power up itsped as generated which the integral circuit RSA. A power up signal is used to trigger soft start elembry that reduces the dary cycle of the switched and person which appears with modulated switch 2RS for a production and pairs with modulated switch 2RS for a production and pairs with modulated switch 2RS for a production and pairs with modulated switch 2RS for a production and pairs with modulated switch 2RS for a production and pairs with a country of expalsing a circuit RSA and pairs with modulated switch 2RS for a production and pairs with a country of the pairs of the pairs

spein.
Alternatively, or in addition to soft start functionality
regulation circuit E30 may also have frequency liber from
historisty. That is, the smitching frequency of the regulation
circuit E30 various according to an internal frequency was
functional E30 various according to an internal frequency was innairy. That is, the smalching frequency of the regularies circuit 800 varies according to an intensal Sequency varia-tion signal. This was advantage over the frequency little operation of FRC 1 in that the frequency range of the presently regulation circuit 830 is known and fand, and is not subject to the line voltage or load magnitude variations.

not subject to the line voltage or load magnitude varieties. Ridewing to FIG. 9, frequency varieties elevait 465 and main oscillator 485 function as described with respect to FIG. 3. In operation is in the varience of the high and low states of marinums days yeals signed 670 that generates the frequency litter functionality of the regulation circuit 350. A proceedity preferred regulation circuit 550 and its nearly-man application of the depicted and described in coperation at depicted and described in coperating used regulation Sec. No. (8/082,520 which is heavy incorpo-

and function to described with respect of FIGS. 6 and 7.

Las son start, mecrocateny or too personny presents regulation circula 130 of PTA. B, will ichorian the on-time of switch 433 to less thon the time of the mechanic day cycle-signal 607 as hope as the soft start cauthe signal 421 is provided and the magnitude of incoracy variation signal 400 is less than the magnitude of main oscillation signal 415.

400 is less than the magnitude of main escillation signal 415. The presently pedered regulation circuit 830 preferably congrises a mondified device.

While the embodiments, applications and advantages of the protect invention leven been depicted and described, there are many, more embodiments, applications and advantages possible without deviating from the april of the invention are not to be estitled to the printage capoliuments, specification or derecing of the transaction to be afforded this patient about therefore only be restricted in accordance with the spirit mid blackedy acops of the following chims.

What is claimed in

- a first terminal:
- s second seconds.
- a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal seconding to a drive signal provided at said control imput;
- an entillator that provides a mach compeleing as on ease and an off-of

- comprising as on state and an off-state;
  a three circuit that provides said are signal according to
  said mississen dety types signal; and:
  a soft state circuit that provides a signal instruction said
  drive circuit to disable said drive signal during all tent
  a portion of said neckates of said maximum duty types.

  2. The pube width inodulated switch of claim 3 wherein
  said a first terminal, and second terminal, said switch, said
  macilitate, said drive circuit and said soft state circuit couprises a mountiblic device.

  3. The pube width misobalated switch of claim 3 further
  comprising an additional occilitate that provides a soft and
  signal to said soft state circuit, and when he were mid soft
  state signal is recurred and soft state circuit ceasing operation.
- 4. The pulse width modulated circuit of claim 3 wherein
  said additional conflictor facility compains

- said additional corditor father comparison signal when a a comparator that provides a comparator signal when a magnitude of a seferance signal is greater than or equal to a congolinda of said frequency variation oscillation signal, and so investor that receives and comparator signal and provides said soft start signal. The public said soft start signal The public with modulated switch of claim I further compelsing a Bequency variation circuit that provides a frequency variation signal, wherein said soft start circuit an excillation signal and wherein said soft start circuit to disable said drive signal when a magnipules of said our little of disable and drive signal when a magnipules of said our little of signal is greater these a sugnitude of said frequency variation agont.
- ages).

  6. The pulse with modelated switch of chim 5 wherein said escillator comprises an input that receives said femiliated securities as the sald oscillator comprises an input that receives said fre-quency signal and raid notification signal comprises a fre-quency range, and whentin said frequency of said carillation

- DC signil from said power supply or second terminal of said first winding or first terminal of said pulse width modules
- and winding magnetically equipled to said first wing, said first winding capable of being complet to

https://www.newpower.com/puresses/ files afgest my wherein a side maximum time perio according to a pagnitude of said facquency variaties 13. The regulation clocult of chiefs 9 fasther cours forchack terminal and wherein wheth a signal is re-said feedback terminal and drive signal is discord

said feedback terminal anid drive algoal is discontinued for at least one cycle.

16. The regulation circuit of claim 9 wherein anid first terminal, said second terminal, said oscillator and said soft start clevial computer 's monoblishe device.

17. The regulation circuit of claim 16 further comprising a convext finit circuit that provides a signal shortering said drive circuit to discontinue said drive signal whom a carroad received at said first terminal of said regulation circuit is above a threshold level.

18. The regulation circuit of claim 9 further comprising

**PX 4** 

# United States Patent 1191

[11] Patent Number:

4,811,075

Eklund

[45] Date of Patent:

Mar. 7, 1989

	[54]	HIGH VO	LTAGE MOS TRANSISTORS
	[75]	Inventor:	Klas H. Eklund, Los Gatos, Calif.
	[73]	Assignees	Pewer Integrations, Inc., Mountain View, Calif.
	[21]	Appl. No.:	41,994
	[22]	Filed:	Apr. 24, 1987
•	βŊ	Ist. Cl.4	HOLL 27/02; HOLL 29/78;
	[52]·	us, a	H01L, 29/80 357/46; 357/22, 357/23.4; 357/23.8
	[58]	Field of Se	357/23.8, 23.4, 46, 357/23.8, 23.4, 46,
	[56]		References Cited
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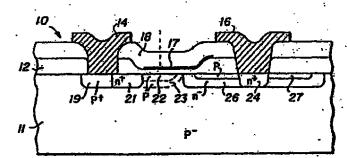
Primary Examiner—Andrew J. James

Assistant Examiner-Jerome Jackson Astorney, Agent, or Furn-Thomas E. Schatzel

37] ABSTRACT

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and mailar to that of the substrate is provided by ion-amplantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

7 Claims, 2 Drawing Sheets





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U.S. Patent

Mar. 7, 1989

Sheet 1 of 2

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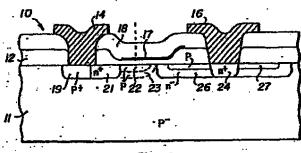
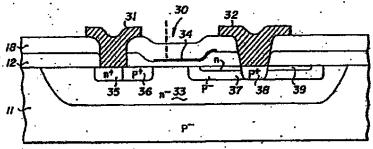
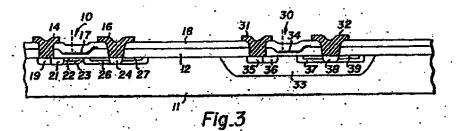


Fig.1



Fig\_2



U.S. Patent

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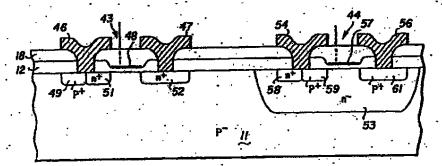
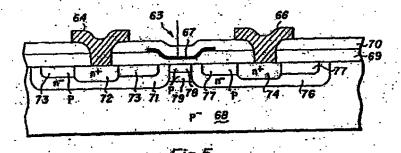


Fig.4



PIF 00005

# 4,811,075

# 1 HIGH VOLTAGE MOS TRANSISTORS

# BACKGROUND OF THE INVENTION

# L Field of the invention

This invention relates generally to high voltage metal-oxide semiconductor (MOS) transistors of the field-effect type. More specifically, the transistors can be made as either discrets or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary maintain on the same chip.

# 2 Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGPET or MOSPET in series with a single sided JPET. Two of such high voltage devices having opposite conductivity typer can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate.

being impeases in me invest in a processor.

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net manber of 30 charges therein. For optimum performance, the net number of charges should be around 1×10<sup>12</sup>/cm<sup>2</sup>, Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the correst capabilities of the devices are poor. The main advantage 15 is that low voltage control logic easily can be combine on the same chip. For these devices, a general figure of ment can be determined by the product of ResA (where Ros is the on-resistance in the linear region and A is the area taken up by the device). For an a-channel device in the voltage range of two hundred fifty to three hundred volts,  $R_{en}xA$  is typically  $10-15~\Omega$  and A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 th man, but is much more difficult to combine with law voltage control 45 logic on the same chip. Thus, the application of these high voltage devices is restricted to correst level below 100 mA, such as display drivers. Even such drivers are more costly due to poor seen efficiency of the high voltage devices.

# SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high 35

Another object of the investion is to provide a high voltage MOS translator that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt a channel device with a figure of merit,  $R_{ob} \times A$ , of about 2.0  $\Omega$  mm<sup>2</sup>,

Briefly, the present invention includes an insulated gate, field-effect transistor (IGFET or MOSFET) and a double-sided junction gate field-effect transistor (IFET) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of 65 the invention, a complementary pair of such high voltage MOS transistors having opposite conductivity type are provided on the same chip.

Advantages of the invention include more efficient high voltage MOS transitors, compatibility with five volt logic, and for an a-channel device, voltage capability of three hundred volts with a figure of merit,  $R_{\rm eff} \propto A$ , of about 2.0  $\Omega$  mm<sup>2</sup>.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

### IN THE DRAWINGS

FIG. 1 is a disgrammatic view of a high voltage MOS transistor of the a-chantel type embodying the present invention.

FIG. 2 is a diagrammatic view of a high voltage MOS transitor of the p-channel type embodying the present invention.

FIG. 3 is a diagrammatic view of the transistors shown in FIGS. 1 and 3 forming a complementary pair on the same chip.

FIG. 4 is a diagrammatic view of low voltage, C-MOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. 3.

FIG. 5 is a diagrammatic view of a symmetric highvoltage a-channel device wherein the source region and the drain region are similar.

# DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. 1, an a-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a slicon dignide layer 12. A metal source contact 14 and a metal dirain contact 16 entend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the dram contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p<sup>+</sup> maintal and a pocket 21 of n<sup>+</sup> material are diffused into the p<sup>-</sup> substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implicit 22 of p-type material for adjusting the threshold voltage and a practit through implient 23 of p-type material for avoiding punch through voltage breakdown. Beneath this drain contact 16, a pocket 24 of n<sup>+</sup> interial is diffused into the substrate. An extended drain region 26 of n-material is formed by diffusion or loss implantation on top of the p-substrate, and extende from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 77 of p-material is provided by ion-implantation through the same mask window as the nate of drain region to cover an intermediate portion thereof, while the end portions of the drain region are nacovered to contact the afficon dioxide layer 12. The top layer is either connected to the substrate or left Receiver.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material is the extended drain region 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (IFET). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a depletion MOS type.

By adding the top layer 27 over the extended drain 10 segion 26 and connecting this top layer to the substrate 11, the net imader of charges in the extended drain region can be increased from 1×10<sup>12</sup>/cm<sup>2</sup> to around 2×10<sup>12</sup>/cm<sup>2</sup>, or approximately double. This drastically rethrees the on-resistance of the transistor 10. The pinch 15 off voltage of the extended drain region can be reduced from typically around forty volts to below an volts. Thus, a conventional short channel, thin gate oxide MoS transistors can be used as the series branketor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually regainers an additional power supply of tent to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type too layer 27 can be made very shallow 30 with a depth of one micron or less, the doping density in that layer will be in the range of 5×10<sup>16</sup>...1×10<sup>17</sup>/cm<sup>3</sup>. At doping levels above 10<sup>16</sup>/cm<sup>3</sup>, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a 35 higher breakdown voltage for fixed geometry. The number of charges is the top layer is around 1×10<sup>12</sup>/cm<sup>3</sup>, and to first order approximation independent of doors.

dent of depth.

The combined benefits of the above features result in 40 a voltage capability of three hundred volts with a figure of merit, R<sub>ev</sub> x A, of about 20 Ω mm² for the transistor 10. Comently used integrated MOS transistors have a figure of merit of about 10-15 Ω mm², while the best discrete vertical D-MOS devices on the market in x 45 similar voltage range have a figure of merit of 3-4 Ω mm².

With reference to FIG. 2, a p-channel type, high woltage MOS translator is indicated generally by reference asserted 38. Since the layers of substrate, afficon 50 dioxide, and insulation for this translator are similar to those previously described for translator 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 13 and a metal drain contact 35 and as metal drain contact 35 and as metal drain contact 35 22 extend through the insulation layer and the silicon dioxide layer to an awell 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrode, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is 60 very thin so that the gate is slightly officet and insulated from the n-well. The gate is slightly officet and insulated from the n-well. The gate is slightly officet and insulated from the n-well. The gate is slightly officet and insulated are covered by the insulation layer 13.

A pocket 35 of a+type material and a pocket 36 of p+type material are provided in the n-well 33 beneath 65 the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from be-

neath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of a-material is provided by ion-implicatation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon djoxide layer i2. The top layer is either connected to the n-well or left floating.

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or left floating.

The gate 34 controls by field-effect the carrent flow the gate 34 controls by field-effect the carrent flow thereander laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be constrolled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFET) connected in series with a double-sided, junction-gate field-effect transistor (IFET). The a-well under the extended drain region has to be depleted before breakdown occurs between the n-drain contact pocket 38 and the n-well.

Looking now at FIG. 3, an n-channel transistor 10, similar to that shown in FIG. 1, and a p-channel transistor 30, similar to that shown in FIG. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to FIGS. 1 and 2, no further description is considered necessary.

As shown in FIG. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 38, shown in FIG. 3. These low voltage devices enable low voltage logic and malog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysision gate 43. A p+ pocket 49 and an n+ pocket 51 are provided in the p- substrate beneath the source contact. The n+ pocket extends to beneath the gate. An n+ pocket 52 is provided beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets \$1 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysiticon gate 57. An at pocket 56 and a pt pocket 59 are progate 57. An at pocket as and a product as he period in the n-well beneath the source contact and a prochet 51 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of a or p type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitacial layer or spi-island that merely supports and can be considered a secondary substrate. An epi-island can be considered a secondary substrate. An epi-island is a portion of an epitacial layer of one conductivity type that is isolated from the remaking portion of the epitacial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

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mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other

FIG. 5 shows a symmetrical x-channel device 63-having a source contact 64 and a drain contact 66. A 5 polysilicus gate 67 is insulated from a substrate 68 by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An a-type extended source region 71 is provided beneath the source contact and an n+ type pocket 72. A top layer 73 of p-type material is 10 positioned over an intermediate portion of the extended source region, while the end portions of the extended source region, waste un can posturate of the service region contact the silicon dixade layer thereshove. Beneath the drain contact is an n+ type pocket 74 and an n-type extended drain region 76. A top layer 15 73 of n-tw 73 of p-type extended drain region 76. A top layer
73 of p-type material is positioned over an intermediate
portion of the extended drain region and end portions of
the extended drain region contact the silicon dioxide
types. As implies 72. The contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region 20 and the extended drain region for instaining the threshold voltage. A similar implant 79 for sextaining the provided the reproductive terms of the provided beautiful to the reproductive terms of the restriction to the restri old voltage. A similar implant 79 for sustaining me punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended down, the source can a extended down, the source can 25. sectain the same high potential as the drain. A symmet-ric p-channel device could be made in a similar way ng opposite conductivity type materials

tring oppose consuctivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transition has a weitinge capability of three hundred volts for an n-channel device, and has a figure of specit;  $R_{\rm eq} \times A$ , of about 2.0  $\Omega_{\rm min}^2$ . The transistor is formed by an insulated-gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either a channel or p channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of apposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be 45 anderstood that such disclosure is not to be interpreted as limiting. Various alterations and modification no doubt become apparent to those of ordinary skill in no other recome apparent or more to consular some interesting read the above disclosure. Accordingly, it is intended that the appended claims be interesting all alterations and modifications as fall within the true spirit and scope of the invention.

- A high voltage MOS transistor comprising:
   a semiconductor substrate of a first conductivity type: 55
- a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source contact connected to one pocket, a drain contact connected to the other pocket, an extended drain region of the second conductivity
- type extending laterally each way from the drain contact pucket in surface edjoining positions, a surface adjoining layer of material of the first con- 65
- ductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage, lating layer on the surface of the substrate and

covering at least that portion between the source contact pocket and the nearest surface adjoining position of the extended drain region, and

- gate electrode on the insulating layer and electrically solated from the substrate region theresader which forms a channel laterally between the source contact pocket and the searest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereinder through the channel.

  2. The high-voltage MOS manistor of claim 1
- said top layer has a depth of one micron or less.

  3. The high-voltage MOS transistor of claim 1
- wateren, said too layer has a doping density higher than 5×10 fcm² so that the mobility starts to degrade.

  4. The high voltage MOS transistor of claim 1 having one channel conductivity type in combination with a complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.
- 5. The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS im-
- plemented device.

  6. The combination of claim 5 further including.
- a complementary high voltage MOS transistor, and a complementary low veltage CMOS implemented device on the same clim and isolated from each
- 7. A high voltage MOS transistor comprising: a semiconductor substrate of a first conductivity type
- a pair of interakly spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
- a source confact connected to one pocket, n extended source region of the second conductivity type extending interally each way from the source contact pocket to surface adjoining positions.
  - contact pocket to surface adjoining positions, a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the entended source region between the surfaceadjoining position
  - said top layer and said substrate being subject to application of a reverse-bias voltage, drain contact connected to the other pocket.
  - at extended dish region of the second conductivity hype extending breathy each way from the drain contact pocket to surface-adjoining positions, a surface adjoining layer of material of the first con-
  - discrivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-offcining positions, said top layer of material and said substrate being subject to application of a reverse-birs voltage,
  - anyles to ephanical or a reversions. Votage, insulating a least that portion between the pearest surface-edicining positions of the extended source region and the extended drain region, and
  - gate electrode on the insulating layer and electri-cally isolated from the substrate region thereunder which forms a channel laterally between the nearreason axions a channel laterally between the next-est surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the cur-rent flow theremet

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# United States Patent 1191

[11] Patent Number:

4,811,075

Ekland

Date of Patent:

Mar. 7, 1989

	[54]	HICH	VOLTA	CE MOS	TRANSISTORS
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- [75] Inventor: Klas H. Eklund, Los Gatos, Calif.
- [73] Assignee: Power lategrations, Inc., Mountain View, Calif.
- [21] Appl. No.: 41,994
- [12] Filed: Apr. 24, 1987
- [51] Let. CL\* ... .... HOLL 27/02; HOLL 29/78; HOHL 29/80
- 357/44; 357/22; 357/23.4; 357/23.8
- . 357/23.**8**, 23.4, 46, 357/22 [58] Field of Search .

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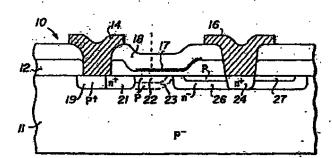
Primary Examiner -- Andrew J. James

Assistant Enquiner-Jerome Jackson Attorney, Agent, or Firm-Thomas E. Schatzel

ABSTRACT .

An insulated-gate, field-effect transistor and a double-An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type oppo-site that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same most window as the extended drain region. This same mask window as the extended drain region. This same mask wantow as the extended craim region. I has top layer covers only an intermediate portion of the extended drain which has each contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the tru layer, which set or other recthrough the extended sum regron can be construct by the substrate and the top layer, which act as gates pro-viding field-effects for pinching off the extended drain region therebetween A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

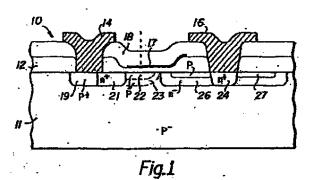
7 Claims, 2 Drawing Sheets

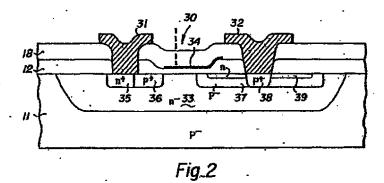


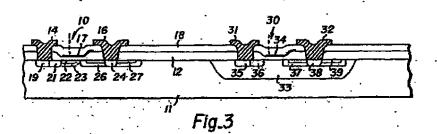
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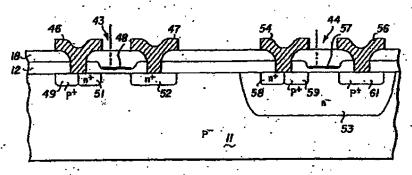
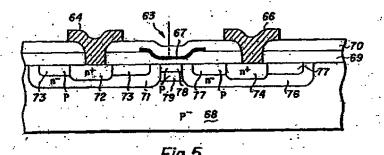


Fig.4



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# HIGH VOLTAGE MOS TRANSISTORS

# BACKGROUND OF THE INVENTION

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# L Field of the Invention

This invention relates generally to high voltage met-al-oxide semiconductor (MOS) transistors of the fieldeffect type. More specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary mannet on the same chip.

 Description of the Prior Art
 Self isolation technology is used for making high
voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is statuted by an 20 clifet gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair on the same chip, with the device having an extended p-type drain being imbedded in an a-well in a p-substrate. The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of

the extended drain region and the net number of to charges thereis. For optimum performance, the net number of charges should be around 1×1012/cm2. Such devices have been used for making display drivers in the one hundred to two hundred volt range, but the current capabilities of the devices are poor. The main advantage 35 is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of ment can be determined by the product of  $R_{\rm opt}A$  (where  $R_{\rm op}$  is the on-resistance in the linear region and A is the area taken up by the device). For an a-chainel at device in the voltage range of two hundred fifty to three hundred wolts,  $R_{\rm co} z A$  is typically 10–15  $\Omega$  mm². A discrete vertical D-MOS device in the same voltage range has a figure of merit of 3 () mm2, but is much more difficult to combine with low voltage control 45 logic on the same chip. Thus, the application of these high voltage devices in restricted to current level below 100 mA, such as display drivers. Even such drivers are more costly due to poor srea efficiency of the high voltage devices.

# SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a

more efficient high voltage MOS transistor.

Another object of the invention is to provide a high 55 voltage MOS transistor that is compatible with five volt

A farther object of the invention is to provide a three andred volt a classed device with a figure of merit, Roux A, of about 2.0 Ω mm²,

Briefly, the present invention includes an insulated te, field-effect transistor (IGFET or MOSFET) and a double sided junction gate field-effect transistor (JFEY) connected in series on the same chip to form a high voltage MOS transistor. In a preferred embodiment of 65 the invention, a complementary pair of such high voltage MOS transitors having opposite conductivity type are provided on the same chip.

Advantages of the invention include more efficient high voltage MOS transistors, compatibility with five volt logic, and for an a-channel device, voltage capability of three hundred volts with a figure of merit, Rev 2 A, of about 2.9  $\Omega$  mm<sup>2</sup>.

These and other objects and advantages of the present invention will no doubt become obvious to those of onlinary skill in the art after having read the following detailed description of the preferred embodiments 10 which are illustrated in the various drawing figures.

## IN THE DRAWINGS

FIG. 1 is a diagrammatic view of a high voltage MOS transistor of the n-channel type embodying the present

FIG. 2 is a diagrammatic view of a high voltage MOS transistor of the p-channel type embodying the present

FIG. 3 is a diagrammatic view of the transistors shown in FIGS. 1 and 2 forming a complementary pair on the same chip.

FIG. 4 is a diagrammatic view of low voltage, CMOS implemented devices that can be combined on the same chip with the complementary pair of high voltage MOS transistors shown in FIG. 3.

FIG. 5 is a diagrammatic view of a symmetric high-voltage n-channel device wherein the source region and the drain region are similar.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at FIG. 1; an n-channel type, high voltage MOS transistor, indicated generally by refercase numeral 18, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal diain contact 16 extend through the silicon dioxide layer to the substrate. A polysiticon gate 17 is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and as insulation layer 19 covers the gate and the silicon dionide layer.

Beneath the source contact 14, a pocket 19 of p+ material and a pocket XI of n + material are diffused into the p substrate II. The pocket 21 extends from be-neath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 23 of p-type material for adjusting the threshold younge and a punch through implant 23 of p-type material for avoiding punch through voltage breakdows. Benesit the drain contact 16, a pocket 24 of m+ material is diffused into the substrate. An extended drain region 26 of a-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p-material is provided by ing-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are necovered to contact the silicon dioxide layer 12. The top layer is either connected to the substrate or left

The gate 17 controls by held-effect the current flow thereunder laterally through the p-type material to the a-type material in the extended threir region 26. Further flow through the extended drain region can be controlled by the substrate II and the top layer 27, which Document 598-2

act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 10 can be considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in series unassion (LOFE) or MONTELL COMPETED in series with a double-sided, junction-gate field-effect transistor (FEE). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should be understood that it could also be a lateral D-MOS or a deplenon MOS type

By adding the top layer 27 over the extended drain 19 gion 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain ion can be increased from 1×10<sup>12</sup>/cm<sup>2</sup> to around  $2\times10^{13}/\text{cm}^3$ , or approximately double. This drastically reduces the on-resistance of the transistor 10. The pinch 15 off voltage of the extended drain region can be reduced. from typically around forty welts to below sea wells.

Thus, a conventional short channel, thin gate exide MOS transistors can be used as the series tran instead of a D-MOS device. This results in the follow- 28 ing benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for tonat MUS transact is typically meet lower man for a D-MOS device (0.7 welts compared to two four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually re- 25 quires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thiss, further reduces the total on resistance.

with a depth of one minron or less, the doping density in that layer will be in the range of  $5 \times 10^{16}$ – $1 \times 10^{17}$ /cm<sup>3</sup>. At doping levels above  $10^{16}$ /cm<sup>3</sup>, the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a 35 higher breakdown voltage for fixed geometry. The number of charges in the top layer is around  $1\times 10^{12}/\text{cm}^2$  and to first order approximation independent deut of depth.

benefits of the above features result in 40 a voltage capability of three hundred volts with a figure of inert, R<sub>en</sub> x A, of about 2.0 Ω ane<sup>2</sup> for the transistor 18. Correctly used integrated MOS transistors have a figure of ment of about 19-15 Ω cms<sup>2</sup>, while the best discrete vertical D-MOS devices on the market in a 45 similar voltage range have a figure of ment of 3-4 Ω.

With reference to FIG. 2, a p-channel type, high voltage MOS transition is indicated generally by reference numeral 39. Since the layers of substrate, silicon 5 dioxide, and insulation for this transistor are nimitar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate 11 is covered by a silicon dioxide layer 12 and an insulation layer 18. A metal source contact 31 and a metal drain contact 35 32 extend through the involution layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysificon gate 34, which is an electrode, is positioned between the source contact and the drain as positioned between the surface costant and the diagram of contact at a location where the silicon dioxide layer is 6 very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of a + type material and a pocket 36 of

p+ type material are provided in the n-well 33 beneath 65 the metal source contact 31. The pocket 36 extents to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from be-

neath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mark as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are sincovered to as to contact the silicon dioxide layer 12. The top layer is either connected to the n-weil or left floating.

The gate 34 controls by field-effect the current flow thereunder laterally through the a-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 37; which act as gates providing field-effects for pinching off the ex-tended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGFET or MOSFEI) connected in series with a double-sided, junction-gate field-effect transistor (JFET). The a-well under the extended drain region has to be depleted before breakdown occurs between the p+ drain contact pocket 38 and the s-well.

Looking now at FIG. 3, an a-channel transistor 19, similar to that shown is FIG. 1, and a p-channel transistor 30, similar to that shown in FIG. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transise has been previously described with reference to As the p-type top layer 27 can be made very shallow 30 FIGS. 1 and 2, no further description is considered

> As shown in FIG. 4, low voltage, C-MOS implented devices 43 and 44 can be combined on the s substrate 11 as the high voltage devices 10 and 30, p-suscrare. It as the legs votinge devices (10 and 34, shown in FIG. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an a-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p+ pocket 49 and an n+ pocket 51 are provided in the p- substricts beneath the source contact. The m+ pocket extends to beneath the gate. An n+ pocket 52 is required the source to the contact The mn+ pocket 52 is provided beauth the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysiticon gate 57. An n\* pocket 58 and a p\* pocket 59 are provided in the n-well beneath the storger contact and a p\* pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insoluted from the n-well and

> extends thereabove between pockets 59 and 61.
>
> It should be noted that the term "substrate" refers to
> the physical material on which a microcircuit is fabrithe physical material on which a microcircuit is fabri-cated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a second-ary substrate. Similarly, if a transistor is fabricated on an epitazini layer or spi-island that merely supports and insulates the transistor, the epitoxial layer or epitaind can be considered a secondary substrate. An epi-island is a portion of an epitanial layer of one conductivity type that is isolated from the remaining portion of the epitazial layer by diffusion pockets of an opposite con-ductivity type. When complimentary transistors are formed on the same chip, the well in which one compli-

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mentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.

FIG. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66: A 5 polyaticon gate 67 is insulated from a substrate 68 by a polysuscen gare of a management as an action dioxide layer 69 and the gate is covered by an insulation layer 28. An n-type extended source region and an action layer 28. 71 is provided beneath the source contact and an n+ type pocket 72. A top layer 73 of p-type material is 10 positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon disode layer thereshove. Beneath the drain contact is an m+ type pocket 74 and an n-type extended drain region 76. A top layer 15 73 of p-type material is positioned over an intermediate portion of the extended drain region and and portions of the extended drain region contact the silicon distribe layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region 20 and the extended drain region for instaining the threshold voltage. A similar implant 78 for sustaining the punch-through voltage is provided teneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using conomisis conductivity type materials. portion of the extended drain region and end portions of sing opposite conductivity type materials.

From the foregoing description, it will be seen that an elficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic; 30 which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred voltage for an inchannel device, and has a figure of merit, Res x A, of about 2.0 furms. The transistor is formed by No. NA, of about 20 times. The transitor is formed by an insulated gain field-effect transitor and a double-sided junction-gate field-effect transitors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage completely in the most and the first later to the conductivity. trol legic on the same chip. Further devices of opposite conductivity can be combined in a complementary man-

die chip. ner on the s

har on une same camp.

Although the present invention has been described in terms of the presently preferred embodiment; it is to be 43 audenstood that such disclosure is not to be interpreted as finiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in no unnot become apparent to tance or ocumary som in the ant after having read the above disclosure. Accord-ingly, it is intended that the appended claims he inter-preted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

L A high voltage MOS transistor comprisings a semiconductor substrate of a first conductivity type: 35 having a surface

a pair of istensity spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface, a source contact connected to one pocket.

a during contact connected to the other pocket, an extended drain region of the accord.commetivity

type extending laterally each way from the drain consist pocket to surface adjoining positions, a surface adjoining layer of material of the first con- 65 ductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface adjoining positions;

said top layer of material and said substrate being subject to application of a reverse-bias voltage, an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface adjoining position of the extended drain region; and

a gate electrode on the insulating layer and electrically isolated from the substrate region thermader which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current durenader through the channel.

2. The high-voltage MOS transistor of claim 1

and top layer has a depth of one micron or less.

3. The high-voltage MOS transistor of claim 1

wheren,
said top layer has a doping density higher than
5×10<sup>16</sup>/cm<sup>2</sup> so that the mobility starts to degrade.
4 The high-voltage MOS transistor of claim 1 having
one channel conductivity type in combination with a
complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same
chip and isolated from each other.
5 The high voltage MOS transistor of claim 1 combined on the same chip with a low voltage CMOS im-

bined on the same chip with a low voltage CMOS im-

picuncated device.

6. The combination of claim 5 further including, a complementary high voltage MOS transistor, and a complementary low voltage CMOS implemented device on the same chip and isolated from each other.

7. A high voltage MOS transistor comprising: a semiconductor substrate of a first conductivity type

having a surface,
a pair of hierally spaced pockets of semiconductor
material of a second conductivity type within the
substrate and adjoining the substrate surface,
a source conduct connected to one pocket,

a source connect connected to one pocket, an extended source region of the accord conductivity type extending intendly each way firms the source contact pocket to surface adjoining positions, a surface adjoining layer of material of the first con-ductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions. adjoining positions.

bication of a reverse-past voltage,

said top layer and said substrate being subject to application of a reverse-bias voltage,
an extended drain region of the second conductivity
lype extending laterally each way from the drain
contact pocket to surface-adjoining positions,
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of
the extended drain region between the drain
contact pocket and the surface-adjoining positions,
said top layer of material and said substrate being
subject to application of a reverse-bias voltage,
an insulating layer on the surface of the substrate and
covering at least that portion between the nearest
surface-adjoining positions of the extended source
region and the extended drain region, and
a gate electrode on the insulating layer and electri-

gate electrode on the insulating layer and electri-cally isolated from the substrate region thereunder which forms a channel laterally between the sear-est surface-adjoining positions of the extended source region and the extended dualn region, said gate electrode controlling by field-effect the cur-rent flow thereunder through the channel.

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170.10 201 G 41994 PATENT

Case Docket No. SS-520-D1

Date \_ April 20, 1987

THE COMMISSIONER OF PATENTS AND TRADEMARKS Washington, B.C. 20231

Transmitted herewith for filing is the patent application of:

Inventor:

Klas H. Eklund

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PATENT

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

To the Commissioner of Patents and Trademerks:

Your petitioner, KLAS H. EKLUND, a citizen of Finland and resident of Los Gatos, California, whose post office address is 243 Mistletce Road; 95030; prays that letters patent may be granted to him for

AN HIGH VOLTAGE MOS TRANSISTORS

set forth in the following specification.

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High Voltage NOS Transistors

# BACKGROUND OF THE INVENTION

# Pield of the Invention

This invention relates generally to high voltage metal-exide semiconductor (NOS) transistors of the field-effect type. Hore specifically, the transistors can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The integrated devices can easily be combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

# Description of the Prior Art

Self isolation technology is used for making high voltage MOS devices, particularly integrated high voltage devices in combination with low voltage control logic on the same chip. The voltage is sustained by an offset gate, as a lightly doped extended drain region is used. Such devices can be considered as an IGPET or MOSFET in series with a single sided JFET. Two of such high voltage devices having opposite conductivity types can be used as a complementary pair, with the same chip, with the device having an extended p-type drain being imbedded in an n-well in a p-substrate,

The voltage capability of such high voltage devices is determined by the doping of the substrate, the length of the extended drain region and the net number of charges therein. For optimum performance,

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the net number of charges should be around 1x1012/cm2. Such devices have been used for making display drivers in the one hundred to two hundred wolk range, but the current capabilities of the devices are poor. The main advantage is that low voltage control logic easily can be combined on the same chip. For these devices, a general figure of merit can be determined by the product of Robat (where Ron is the on-resistance in the linear region and A is the area taken up by the device). For an m-channel device in the voltage range of two hundred fifty to three hundred volts, RonzA is typically 10 - 150 mm<sup>2</sup>. A discrete vertical D-MOS device in the same voltage range has a figure of merit of 30 mm2, but is much more difficult to combine with low voltage control logic on the same chip. Thus, the application of these high voltage devices is restricted to current level below 180 mA, such as display drivers. Even such drivers are more costly due to poor area efficiency of the high voltage čevices.

## SUMMARY OF THE PRESENT INVENTION

An object of the present invention is to provide a more efficient high voltage MOS transistor.

Another object of the invention is to provide a high voltage MOS transistor that is compatible with five volt logic.

A further object of the invention is to provide a three hundred volt n-channel device with a figure of merit,  $R_{\rm on} \propto A_{\rm r}$  of about 2.0  $\Omega \, {\rm min}^2$ ,

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Fig. 4 is a diagrammatic view of low voltage. C-MOS implemented devices that can be combined on the same thip with the complementary pair of high voltage MOS transistors shown in Fig. 3.

Fig. 5 is a diagrammatic view of a symmetric high-voltage m-channel device wherein the source region and the drain region are similar.

# DESCRIPTION OF THE PREFERRED EMBODIMENT

Looking now at Fig. 1, an n-channel type, high voltage MOS transistor, indicated generally by reference numeral 10, is formed on a p-substrate 11 covered by a silicon dioxide layer 12. A metal source contact 14 and a metal drain contact 16 extend through the silicon dioxide layer to the substrate. A polysilicon gate 17 is positioned between the source contact and the drain contact at a location where the silicon diexide layer is very thin so that the gate is slightly offset and insulated from the substrate. The polysilicon gate is the gate electrode, and an insulation layer 18 covers the gate and the silicon dioxide layer.

Beneath the source contact 14, a pocket 19 of p+ material and a pocket 21 of n+ material are diffused into the p substrate 11. The pocket 21 extends from beneath the source contact to the gate 17. Beneath the gate is a threshold voltage implant 22 of p-type material for adjusting the threshold voltage and a punch through implant 23 of p-type material for avoiding punch through voltage breakdown. Beneath the drain contact 15, a pocket 24 of nt material is diffused into the substrate. An

extended drain region 26 of n-material is formed by diffusion or ion implantation on top of the p-substrate, and extends from beneath gate 17 to the pocket 24 and a similar distance to the opposite side of the pocket. A top layer 27 of p-material is provided by ion-implantation through the same mask window as the extended drain region to cover an intermediate portion thereof, while the end portions of the drain region are uncovered to contact the silfcon dioxide layer 12. The top layer is either connected to the substrate or left floating.

The gate 17 controls by field-effect the current flow thereunder laterally through the p-type material to the n-type material in the extended drain region 15 26. Further flow through the extended drain region can be controlled by the substrate 11 and the top layer 27, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 16 can be. considered as an insulated gate, field-effect transistor (IGFET or MOSFET) connected in meries with a double-sided, junction-gate field-effect transistor (JFST). While the insulated gate, field-effect transistor shown is a conventional MOS type, it should 25 be understood that it could also be a lateral D-MOS or a depletion HOS type.

By adding the top layer 27 over the extended drain region 26 and connecting this top layer to the substrate 11, the net number of charges in the extended drain region can be increased from  $1 \times 10^{12}/cm^2$  to around  $2 \times 10^{12}/cm^2$ , or approximately double. This drastically reduces the on-resistance of the transistor 16. The pinch off

voltage of the extended drain region can be reduced from typically around forty volts to below ten volts. Thus, a conventional short channel, thin gate oxide MOS transistors can be used as the series transistor instead of a D-MOS device. This results in the following benefits. First, the threshold voltage of a conventional MOS transistor is typically much lower than for a D-MOS device (0.7 volts compared to two-four volts for the D-MOS device) and thus, is directly compatible with five volt logic. The D-MOS device usually requires an additional power supply of ten to fifteen volts for driving the gate. Second, the conventional MOS transistor has less on resistance and thus, further reduces the total on resistance.

As the p-type top layer 27 can be made very shallow with a depth of one micron or less, the doping density in that layer will be in the range of  $5 \times 10^{16} - 1 \times 10^{17}/\mathrm{cm}^3$ . At doping levels above  $10^{16}/\mathrm{cm}^3$ , the mobility starts to degrade and a decrease in mobility will increase the critical electrical field for breakdown, thus giving a higher breakdown voltage for fixed geometry. The number of charges in the top layer is around  $1 \times 10^{12}/\mathrm{cm}^2$  and to first order approximation independent of depth.

The combined benefits of the above features result in a voltage capability of three hundred volts with a figure of marit,  $R_{\rm OR} \times A$ , of about 2.0  $\Omega$  mm<sup>2</sup> for the transistor 10. Currently used integrated MOS transistors have a figure of merit of about 10 - 15  $\Omega$  mm<sup>2</sup>, while the best discrete vertical D-MOS devices on the market in a similar voltage range have a figure of merit of 3 - 4 $\Omega$  mm<sup>2</sup>.

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With reference to Fig. 2, a p-channel type, high voltage MOS transistor is indicated generally by reference numeral 30. Since the layers of substrate, silicon dioxide, and insulation for this transistor are similar to those previously described for transistor 10, they will be given like reference numerals. A p-substrate II is covered by a silicon dioxide layer 12 and am insulation layer 18. A metal source contact 31 and a metal drain contact 12 extend through the insulation layer and the silicon dioxide layer to an n-well 33 that is embedded in the substrate. A polysilicon gate 34, which is an electrods, is positioned between the source contact and the drain contact at a location where the silicon dioxide layer is very thin so that the gate is slightly offset and insulated from the n-well. The gate and the silicon dioxide layer are covered by the insulation layer 18.

A pocket 35 of n\* type material and a pocket 36 of p+ type material are provided in the n-well 33 beneath the metal source contact 31. The pocket 36 extends to the gate 34. An extended drain region 37 of p-type material is formed in the n-well and extends from beneath the gate to a pocket 38 located beneath the drain contact 32, and the extended drain region continues a similar distance on the opposite side of the drain contact. A top layer 39 of n-material is provided by ion-implantation through the same window of the mask as the extended drain region to cover an intermediate portion thereof. The end portions of the extended drain region are uncovered so as to contact the silicon dioxide layer 12. The top layer is either connected to the n-well or left floating.

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The gate 34 controls by field-effect the current flow thereunder laterally through the n-type material to the p-type material in the extended drain region 37. Further flow through the extended drain region can be controlled by the n-well 33 and the top layer 39, which act as gates providing field-effects for pinching off the extended drain region therebetween. Thus, the transistor 30 can be considered as an insulated-gate field-effect transistor (IGPET or MOSPET) connected in series with a double-sided, junction-gate field-effect transistor (JTET). The n-well under the extended drain region has to be depleted before breakdown occurs between the p through the contact pocket 38 and the n-well.

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Looking now at Fig. 3, an n-channel transistor 10, similar to that shown in Fig. 1, and a p-channel transistor 30, similar to that shown in Fig. 2, are shown as a complementary pair on the same substrate 11 and isolated from each other. Since the details of each transistor has been previously described with reference to Figs. 1 and 2, no further description is considered necessary.

As shown in Fig. 4, low voltage, C-MOS implemented devices 43 and 44 can be combined on the same p-substrate 11 as the high voltage devices 10 and 30, shown in Fig. 3. These low voltage devices enable low voltage logic and analog function to control the high voltage devices. The device 43 is an n-channel type having a source contact 46, a drain contact 47 and a polysilicon gate 48. A p<sup>+</sup> pocket 49 and an n<sup>+</sup> pocket 51 are provided in the p<sup>-</sup> substrate beneath the source contact. The n<sup>+</sup> pocket extends to beneath the gate. As n<sup>+</sup> pocket 52 is provided

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beneath the drain contact. The gate 48 is insulated from the substrate by the silicon dioxide layer 12, but the gate controls the current flow through the substrate between pockets 51 and 52. The gate is covered by the insulation layer 18. An n-well 53 is provided in the substrate to accommodate the low voltage, p-channel device 44. This device includes a source contact 54, a drain contact 56 and a polysilicon gate 57. An n+ pocket 58 and a p+ pocket 59 are provided in the n-well beneath the source contact and a pt pocket 61 is provided in the n-well beneath the drain contact. The gate 57 is insulated from the n-well and extends thereabove between pockets 59 and 61.

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All Fig. 5 shows a symmetrical n-channel device 63 having a source contact 64 and a drain contact 66. A polysiticon gate 67 is insulated from a substrate 58' by a silicon dioxide layer 69 and the gate is covered by an insulation layer 20. An n-type extended source region 71' is provided beneath the source contact and an n+ type pocket 72. A top layer 73 of p-type material is positioned over an intermediate portion of the extended source region, while the end portions of the extended source region contact the silicon dixods layer thereabove. Beneath the drain contact is an n\* type pocket 74 and an n-type extended drawn region 76. A top layer 72 of p-type material is positioned over an intermediate portion of the extended drain region and end portions of the extended drain region contact the silicon dioxide layer. An implant 78 of the p-type material is provided under the gate 67 between the extended source region and the extended drain region for sustaining the threshold voltage. A similar implant 79 for sustaining the

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punch-through voltage is provided beneath the implant 78. Since the symmetrical channel device has both an extended source an an extended drain, the source can sustain the same high potential as the drain. A symmetric p-channel device could be made in a similar way using opposite conductivity type materials.

From the foregoing description, it will be seen that an efficient, high voltage MOS transistor has been provided. This transistor is compatible with five volt logic which easily can be integrated on the same chip. The transistor has a voltage capability of three hundred volts for an a-channel device, and has a figure of merit, Ron x A, of about 2.0 2mm2. The transistor is formed by an insulated gate field-effect transistor and a double-sided junction-gate field-effect transistor connected in series on the same chip. These transistors can be made as either discrete devices or integrated devices of either n-channel or p-channel conductivity. The integrated devices can be easily combined with low voltage control logic on the same chip. Further devices of opposite conductivity can be combined in a complementary manner on the same chip.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those of ordinary skill in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all

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alterations and modifications as fall within the true spirit and scope of the invention.

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## IN THE CLAIMS

- A high-voltage MOS transistor comprising an insulated-gate field-effect transistor, and a double-sided junction-gate field-effect transistor connected in series, said transistors being united in one structure.
- 2. In a high-voltage MOS transistor paving a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the 10 insulated-gate device and the drain, said extended drain region being formed on material having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having 15 a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity type opposite that of the extended drain region, said top layer of material and 20 said material beneath the extended drain region being interconnected with the source for applying a raverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conduct/vity-type materials.
  - source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated gate device and the drain, said extended drain region being formed on material baving a

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conductivity-type opposite that of the extended drain region, and a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

4. The by voltage MOS transistor of claim 1 further including

another high-voltage MOS transistor of opposite conductivity-type forming a complementary pair on the same chip.

5. The high-voltage MOS transistor of claim 2 wherein,

said layer on top of the extended drain region is an ion-implantation.

The high-voltage MOS transistor of claim A

said top layer has a depth of one micron or

7.3 The high-voltage MOS transistor of claim 5/17

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said top layer has a doping density higher than 5 x  $10^{16}/\text{cm}^3$  so that the mobility starts to degrade.

5. The high-voltage NOS transistor of claim 3 wherein.

said extended drain is made of n-type conductive material and said top layer is made of p-type conductive material.

The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of p-type conductive material and said top/layer is made of n-type conductive material.

10. The high-voltage hos transistor of claim 9 wherein,

'said translator is embedded in a well of n-type conductive material in a substrate of p-type conductive material, and further including a complementary high-voltage MOS transistor having an extended drain of n-type conductive material embedded in the substrate.

The high-voltage HOS transistor of claim 3 wherein

both the extended drain region and the top layer of material are diffusions or ion implantations into a substrate or epitaxial layer.

12. The high-voltage MOS transistor of claim 1/1 wherein,

swid extended drain region and the yop layer of material are formed by using the same maps (self alignment).

13. The high-voltage MOS transistor of claim 3 wherein,

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the material on which the extended drain region is formed is a substrate; and

the substrate is of one conductivity-type material, and further including a complementary 15 transistor embedded in a well or epi-island of opposite conductivity-prop naterial on the same substrate.

14. The complementary pair of high-voltage MOS transistors of claim 13 wherein,

the well in which the complementary transistor is embedded is the same diffusion as the extended drawn for the other transistor.

15. The complementary pair of high-voltage MOS transistors of claim 14 wherein,

the well is an n-well and further used for a low vol/rage p-channel device.

16. The high-voltage MOS transistor of claim 2

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the top layer is floating.

17. The high-voltage NOS translator of claim 3

wherein

the source region and the drain region are ormed in a similar manner.

18. The light voltage NOS transistor of claim 3

low voltage logic and analog, function on the

same chip.

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### ABSTRACT OF THE DISCLOSURE

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

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# DECLARATION AND POWER OF ATTORNET FOR PATENT APPLICATION

As a below used inventor, I heraby declare that:

My residence, post office address and citizenship are as stated below next to ap name,

I believe I am the original, first and sole inventor (if only one name is listed below) or am original, first and joint inventor (if plure) names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention contilled:

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